PRELIMINARY

TF90LVDS105

400 Mbps 1:4 LVDS Fanout Buffer with LVCMOS Input

TELEFUNKEN Semiconductors

Features

- **DC to 400 Mbps / 200 MHz low noise, low skew, low power operation**
  - **200 ps (max) channel-to-channel skew**
  - **100 ps (max) pulse skew**
  - **25 mA (max) power supply current**
- **LVDS outputs meet or exceed requirements of ANSI TIA/EIA-644-A standard**
- **Per channel output enable pins minimize power consumption when a channel is not in use**
- **Guaranteed operation within industrial temperature range-40° to +85°C**
- **Available in space saving SOIC-16 and TSSOP-16 packages**
- **Pin compatible with SN65LVDS105**

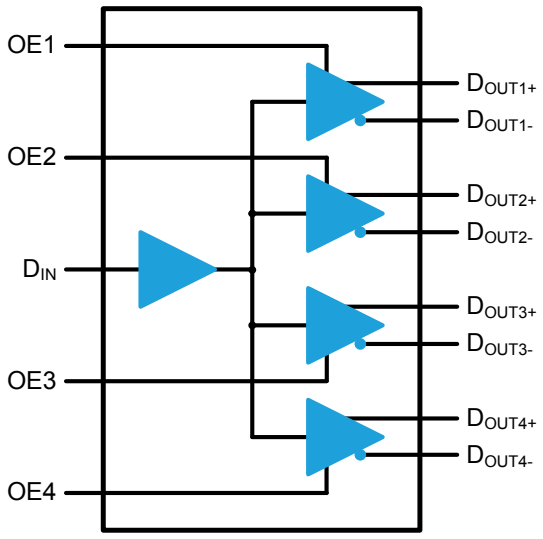
Description

The TF90LVDS105 is a 400 Mbps 1:4 LVDS (low voltage differential signaling) Fanout Buffer optimized for high-speed, low power, low noise transmission over controlled impedance (approximately 100Ω) transmission media (e.g. cables, printed circuit board traces, backplanes).

The TF90LVDS105 accepts a single LVCMOS signal and creates four copies of the signal with LVDS levels. Each differential output can be disabled and put in a high-impedance state via its dedicated enable pin.

Supply current is 25 mA (max). LVDS outputs conform to the ANSI/EIA/TIA-644-A standard. The TF90LVDS105 is offered in 16-pin SOIC and TSSOP packages and operates over an extended -40 °C to +85 °C temperature range.

Function Diagram



TF90LVDS105

Applications

- Digital Copiers
- Wireless Base Stations
- Telecom / Datacom
- Network Routing
- Clock Distribution

SOIC-16(N)

TSSOP-16

Ordering Information

Year Year Week Week

PART NUMBER	PACKAGE	PACK / Qty	MARK
TF90LVDS105-TBU	SOIC-16	Tube / 48	TF YYWW TFS105TB Lot ID
TF90LVDS105-TBG	SOIC-16	T&R / 500	
TF90LVDS105-6CU	TSSOP-16	Tube / 94	TF YYWW TFS1056C Lot ID
TF90LVDS105-6CG	TSSOP-16	T&R / 1000	

Notes

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