TELEFUNKEN
Semiconductors

TF112

7 Port Multidrop IEEE 1149.1 (JTAG) Multiplexer

Features

- **ATPG support from all major vendors**
- **Fully pin and function compatible with NSC SCANSTA112**
- **Muxes 7 local JTAG ports from 1 source**
- **Supports multidrop addressing**
- **Backplane Port and LSP0 can act as slave/master for multi-master operation**
- **Supports live insertion**
- **Transparent Mode for simplified FPGA/CPLD programming**
- **Pass-thru bits can be driven by pins or internal registers to assist Flash Programming**

Applications

- Muxing multiple Scan Chains
- System Level JTAG Test and Programming
- Multidrop and Hierarchical Scan Path Management

Description

The TF112 combines a 7 port IEEE1149.1 (JTAG) multiplexer with addressable multi-drop capability. As a multiplexer, 7 local ports allow partitioning of scan chains to simplify and accelerate programming and test and debug sequences. Optional daughter cards or ICs are easily handled with dedicated scan chains. Local chains can be selected individually or in combination as required.

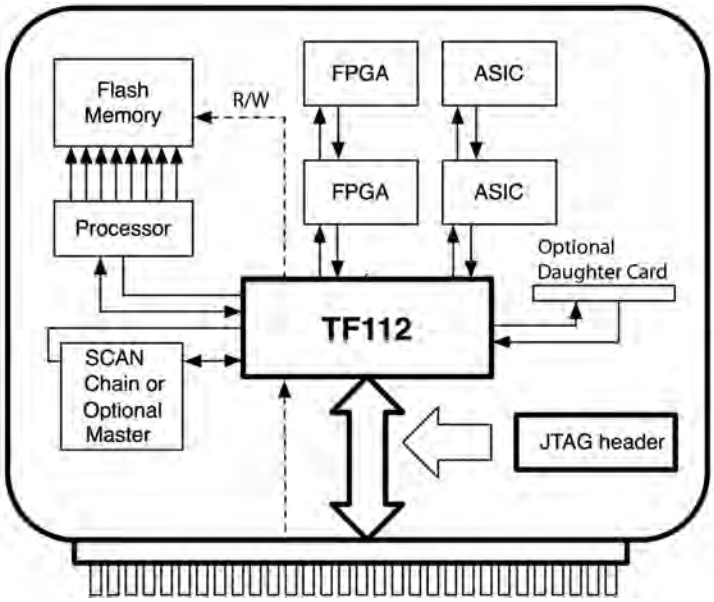
Addressable multi-drop capability allows operation on a backplane with other TF112s or similar addressable devices. 8 address pins are used to set the unique device address. Addressing the device is accomplished by loading the instruction register with a value matching the address pins. The backplane port and one of the local ports are bi-directional and may be set as master or slave. This feature enables multi-master operation.

All major ATPG vendors support this function and both addressing and selection of local ports is handled automatically by the vector generation software.

BGA-100

TQFP-100

Function Diagrams



Ordering Information

Year Year Week Week

PART NUMBER	PACKAGE	PACK / Qty	MARK
TF112-BBV	BGA-100	Tray, 240	TF YYWW TF112 Lot ID
TF112-PBV	TQFP-100	Tray, 90	TF YYWW TF112 Lot ID

Block Diagram

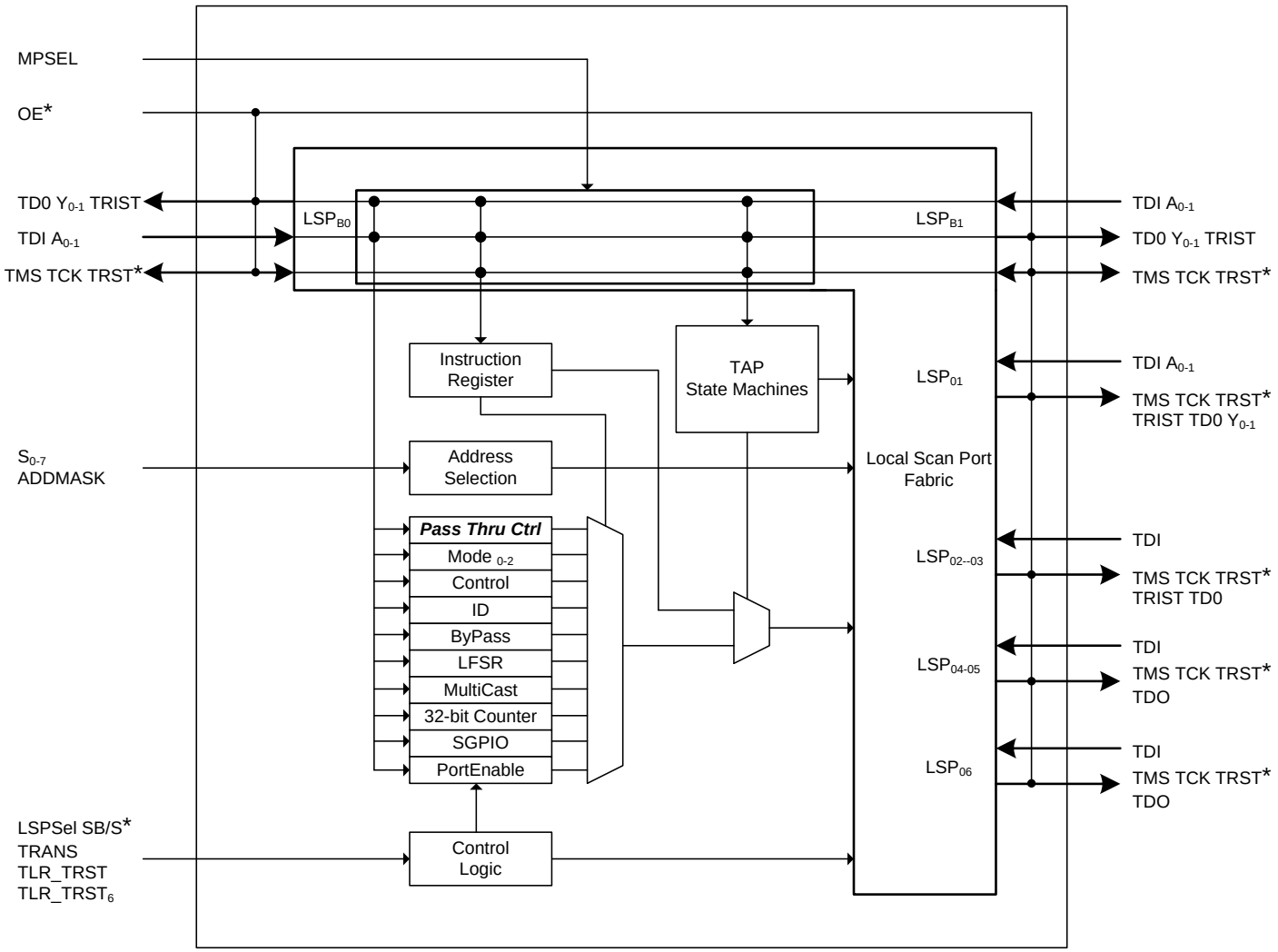


Figure 1. TF112 Block Diagram

Overview

Since its introduction in 1990, the IEEE1149.1 standard (JTAG) has become pervasive in complex digital hardware. In addition to structural test, the standard is now used extensively for tasks such as programming and emulation. These additional uses, along with the increase in complexity and pincount of FPGAs and ASICs, requires effective partitioning of scan chains to minimize test and programming time. The use of scan path multiplexers such as the TF112, enable the configuration of scan chains in an optimal manner. The seven local scan ports (LSPs) also provide a convenient way to provide scan access to optional daughter cards or ASICs. JTAG is also used in fielded platforms for in-situ test and programming. System level JTAG requires the ability to address cards in a multidrop environment and this is accomplished using the de facto industry standard SCAN Bridge addressing scheme. Devices such as the TF112 are completely compatible on a multidrop backplane with other devices using the same scheme.

Addressing TF112 devices and the vector sequence required to select LSPs is an automated process and handled by commercial ATPG software products.

Architecture

A basic block diagram of the TF112 is shown in Figure 2. The functional blocks are as follows:

The TDI/TDO Crossover Master Slave Logic defines the bi-directional B0 and B1 ports as Master and Slave as controlled by MPsel.

The Selection Control Block compares the device address as set by pins S0 thru S7, with the address entered into the instruction register and determines if the TF112 is selected. A selected device is then ready for further instructions; non-selected devices remain in standby.

The TAP Controller is the IEEE1149.1 standard Test Access Port. This 16 state-machine controls the instructions, functionality and timing relationships as defined by the standard.

The Local Scan Port Network is the primary multiplexer that selects individual or combinations of local scan ports. Each local port includes the complete 5 pin boundary scan signal suite.

BGA Connection Diagram

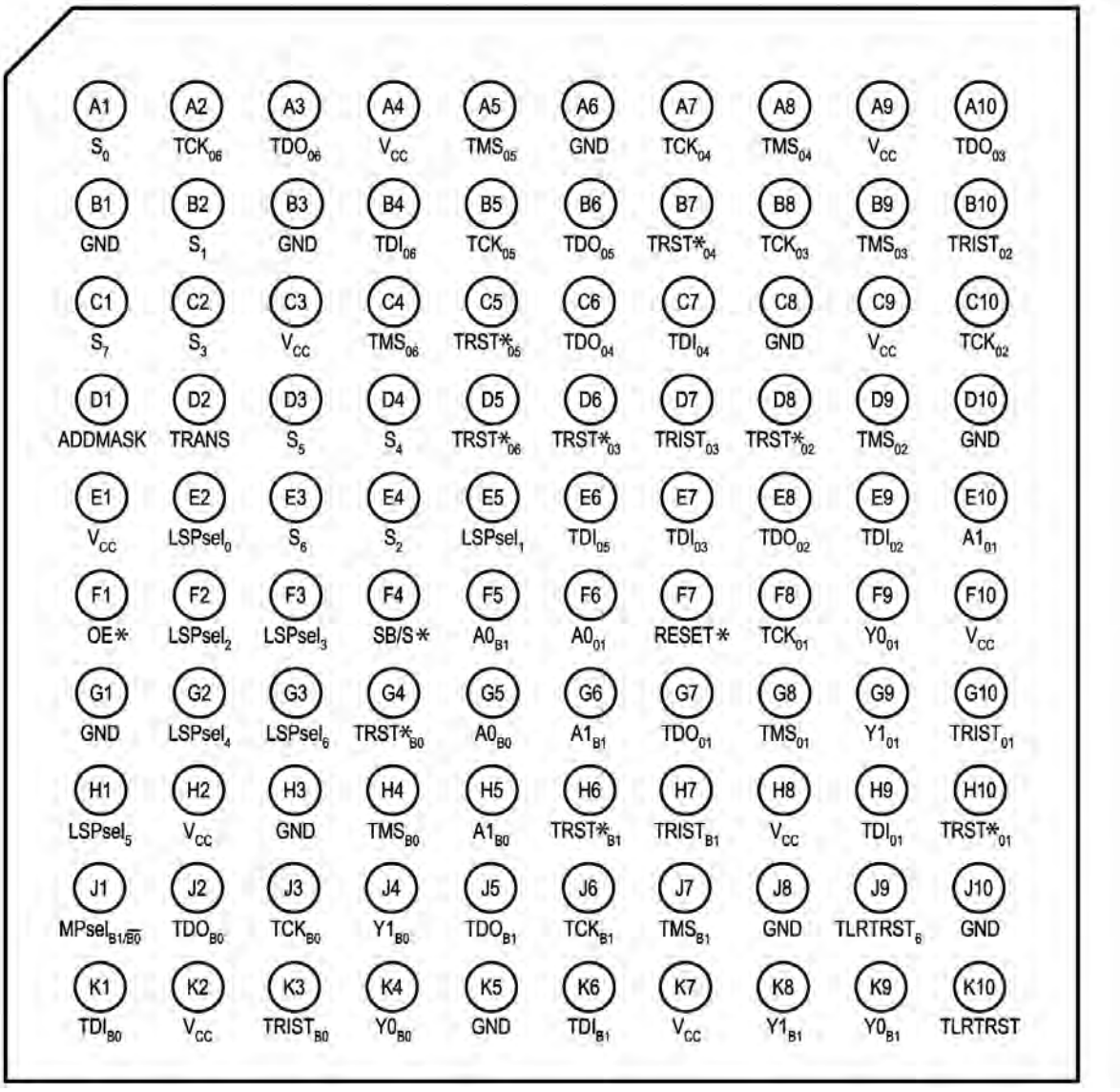


Figure 2. BGA Top View

TQFP Connection Diagram

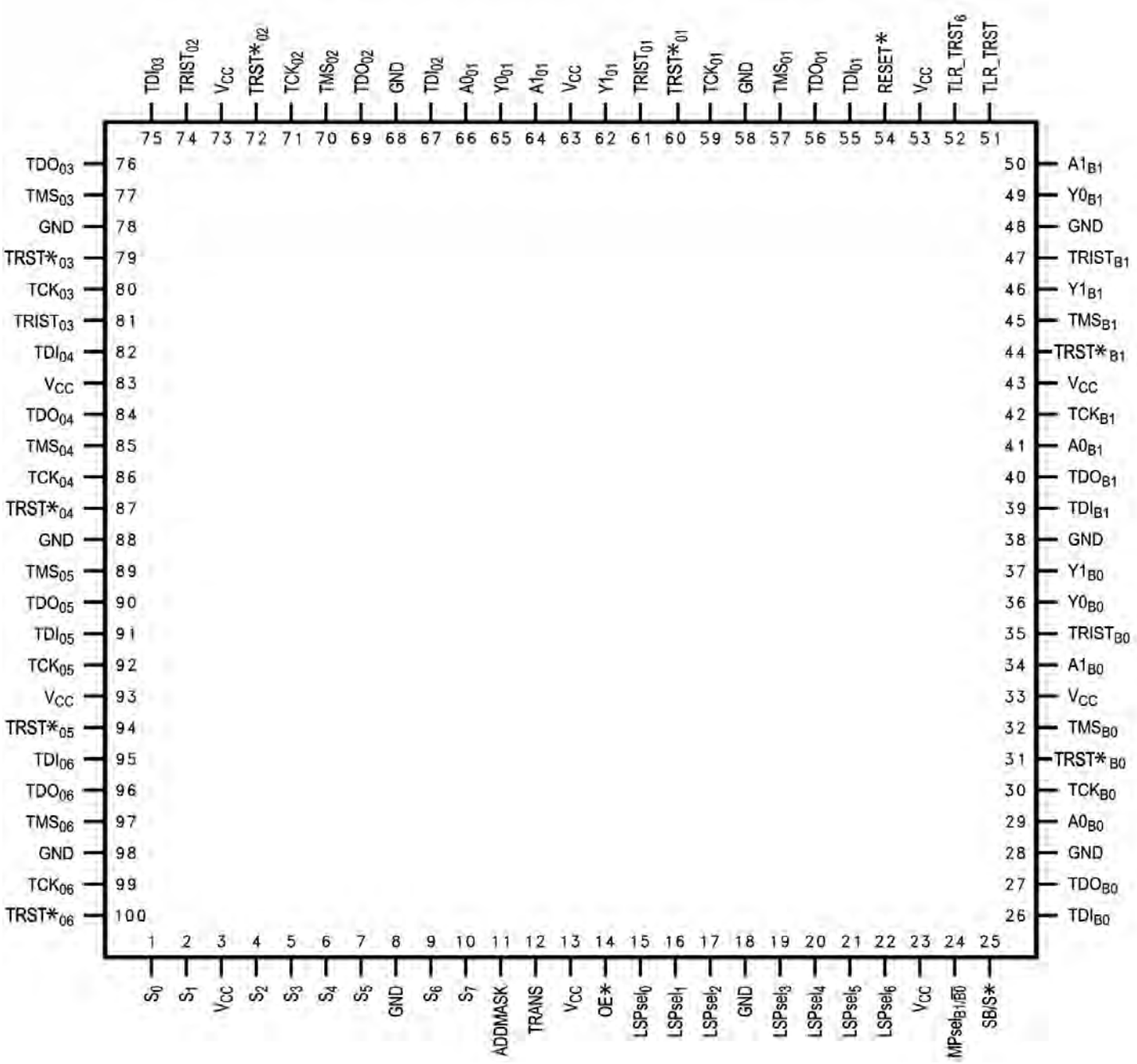


Figure 3. TQFP Top View

Pin Description

Pin Name	No. Pins	I/O	Description
VCC	10	N/A	Power
GND	10	N/A	Ground
RESET*	1	I	Forces an asynchronous reset of the device
ADDMASK	1	I	When asserted, address pins S6 and S7 are masked. This feature is intended for applications where it is desirable for a local master to use the smaller address space and the full address is used at the system level.
MP_{sel}	1	I	Master Port Selection. Determines if LSP_{B0} or LSP_{B1} is the Master port. The non-selected port becomes LSP_{00} . A logic LOW selects LSP_{B0} as master Port
SB/S*	1	I	Selects ScanBridge (logic HIGH) or Stitcher Mode (logic LOW)
$LSP_{sel(0-6)}$	7	I	In stitcher mode, these pins select LSPs for inclusion in the Scan chain.
TRANS	1	I	When the TF112 is to be used in the Stitcher configuration, setting the TRANS pin with a logic HIGH will place the device in Transparent Mode. Transparent mode eliminates the registers and pad bits in the scan chain providing a simpler but generally slower scan path.
TLR_TRST	1	I	This pin can be used to set the TRST* value of LSPs (0-5) over-riding the state machine logic. This feature is included to accommodate non-compliant IEEE1149.1 devices where TRST* must remain HIGH.
TLR_TRST_6	1	I	This pin can be used to set the TRST* value of LSP6 over-riding the state machine logic. This feature is included to accommodate non-compliant IEEE1149.1 devices where TRST must remain HIGH.
TDI_{B0} TDI_{B1}	2	I	This is the Master Test Data Input as described by IEEE1149.1 and includes a 25K ohm internal pull-up. MPsel determines if port B0 or B1 is the master with the non-selected port becoming LSP0. When the device is powered-down this pin is high impedance.
TMS_{BO} TMS_{B1}	2	I/O	This is the Master Test Mode Select as described by IEEE1149.1. The input includes a 25K ohm internal pull-up. MPsel determines if port B0 or B1 is the master with the non-selected port becoming LSP0. When the device is powered-down this pin is high impedance.
TDO_{B0} TDO_{B1}	2	O	This is the Master Test Data Output as described by IEEE1149.1 and has 12 mA drive current. MPsel determines if port B0 or B1 is the master with the non-selected port becoming LSP_0. When the device is powered-down this pin is high impedance.
TCK_{B0} TCK_{B1}	2	I/O	This is the Master Test Clock as described by IEEE1149.1. MPsel determines if port B0 or B1 is the master with the non-selected port becoming LSP_0. When the device is powered-down this pin is high impedance.
$TRST*_{B0}$ $TRST*_{B1}$	2	I/O	This is the Master Test Reset as described by IEEE1149.1. MPsel determines if port B0 or B1 is the master with the non-selected port becoming LSP_0. When the device is powered-down this pin is high impedance

Pin Description (Continued)

Pin Name	No. Pins	I/O	Description
$Y0_{B0}Y1_{B0}Y0_{B1}Y1_{B1}$	4	O	Master Pass-through Outputs. General purpose outputs which are driven by the corresponding input of the selected LSP. (not available when multiple LSPs are selected). There is also an override instruction available in which case the outputs of LSP_0 are controlled by the contents of an internal register. These outputs have 12 mA current drive. MPsel determines if port B0 or B1 is the master with the non-selected port becoming LSP_0.
$A0_{B0}A1_{B0}A0_{B1}A1_{B1}$	4	I	Master Pass-through Inputs. General purpose inputs which are driven to the Yn outputs of the selected LSP. (not available when multiple LSPs are selected). These pins include 25K ohm pull-up resistors. MPsel determines if port B0 or B1 is the master with the non-selected port becoming the LSP_0
$TRIST_{B0}TRIST_{B1}$ $TRIST_{(1-3)}$	5	O	This signal is asserted high when the corresponding TDO is high-impedance. This feature is included to support alternative physical layers where TRIST would enable/disable an external translator
$S_{(0-7)}$	8	I	These 8 inputs set the TF112 address used for addressing in a multidrop environment
OE*	1	I	When HIGH this control signal sets the LSPs in high-impedance. This feature enables the LSPs to be driven by an alternate resource.
$TDO_{(1-6)}$	6	O	Test Data Out as defined by IEEE1149.1 for each of the LSPs. These outputs have 12 mA drive.
$TDI_{(1-6)}$	6	I	Test Data In as defined by IEEE1149.1 for each of the LSPs. These inputs have a 25K ohm internal pull-up.
$TMS_{(1-6)}$	6	O	Test Mode Select as defined by IEEE1149.1 for each of the LSPs. These outputs have 24mA of drive current.
$TCK_{(1-6)}$	6	O	Test Clock as defined by IEEE1149.1 for each of the LSPs. These outputs have 24mA of drive current.
$TRST^*_{(1-6)}$	6	O	Test Reset as defined in IEEE1149.1 for each of the LSPs. These outputs have 24mA of drive current.
$A0_0$,$A1_1$	2	I	Local Pass-through Inputs. General purpose inputs which are driven to the corresponding master Yn output. (not available when multiple LSPs are selected). These pins include 25K ohm pull-up resistors.
$Y0_1Y1_1$	2	O	Local Pass-through Outputs. General purpose outputs which are driven by the corresponding A1 input of the selected Master. There is also an override instruction available in which case the outputs of LSP1 are controlled by the contents of an internal register. (not available when multiple LSPs are selected). These outputs have 12 mA current drive.

Application Overview

The IEEE1149.1 (JTAG) standard has become pervasive in complex digital systems and used for a variety of tasks. The TF112 is a flexible and configurable device enabling efficient and cost effective implementation of JTAG for test, programming and debug. A critical element of cost effective JTAG is the use of software tools for Auto-Test-Pattern-Generation (ATPG) and diagnostics. The TF112 architecture is an established industry de facto standard and supported by all major ATPG engines. Essential elements of the device operation such as addressing and selection of Local Scan Ports (LSPs) is handled in ATPG. Thus only a general knowledge of the device function is necessary, the specific addressing and LSP selection protocol is handled by the software tools.

The IEEE1149.1 standard describes a serial chain encompassing as many devices as required. However in complex systems a single serial chain is grossly inadequate and inefficient. The TF112 includes two methods of creating multiple chains, those being addressability and scan path muxing. The TF112 only responds to its specific address and the 8 external address bits provide 249 unique addresses, along with several multicast addresses. Multidrop addressing is generally used in backplanes where a TF112 on each card is given a unique address. Each card can then be individually accessed by embedded or external JTAG masters. In addition to multidrop addressing, the TF112 is also a scan path mux supporting up to 7 individual chains or LSPs. (Local-Scan-Ports) Typically the multidrop addressing is used to access a specific card and then the mux functionality used to support multiple chains on a card.

The TF112 has two operational modes, those being "SCANBridge" mode, typically supported by ATPG, and "Stitcher" mode, where device functionality is established by external pins. Stitcher mode is often useful in a lab or development setting where ATPG tools and vectors may not yet be available.

The TF112 support both individual addressing and broadcast/multicast addressing operations. During individual addressing operation the master's port TDO_{Bn} is active. During broadcast/multicast addressing operations the master's port TDO_{Bn} is inactive.

ScanBridge Mode

In ScanBridge mode device addressing and LSP selection are typically handled automatically using ATPG tools. ScanBridge mode uses pad bits and internal registers and thus generally provides the fastest test and programming capability.

Transparent Mode

IEEE1149.1 is a synchronous serial vector set. To optimize timing relationships and thus support higher TCK clock rates, the TF112 when in normal operation, inserts pad bits in the scan path. These additional bits are accounted for in the ATPG vector sets and therefore not observed by the user, provided a major commercial ATPG package is generating the vectors. In instances where ATPG is not used it may be desirable to remove these additional bits and simply buffer the IEEE1149.1 signals from the master port to the selected LSP(s). This is known as Transparent mode and is available in ScanBridge mode via an instruction and Stitcher mode using the TRANS pin.

Multiple Master

The TF112 includes a multi-master capability where the master port can be either B0 or B1 with the non-master port then becoming LSP0. This feature is controlled by the MPsel pin and is included to assist with multimaster operation where vectors may be imported over the backplane, from a local embedded master or thru an external source such as ATE.

Pass-Thru Bits

Pass-thru bits are provided to assist with tasks such as Flash programming where external control of Read/Write may be desired. The TF112 pass-thru outputs are driven by the corresponding Master input port unless the Override instruction (0xBF) is loaded, in which case the outputs are controlled by the contents of a register. Upon a POR or TRST, the Enable and Data bits will be set to the default, logic 0. If the Enable is then set to a logic 1, then the Pass-thru output will be controlled by the corresponding register value.

Bit	Default	Function
0	0	LSP0 Y_0 Data bit
1	0	Enable LSP0 Y_0 as GPIO
2	0	LSP0 Y_1 Data bit
3	0	Enable LSP0 Y_1 as GPIO
4	0	LSP1 Y_0 Data bit
5	0	Enable LSP1 Y_0 as GPIO
6	0	LSP1 Y_1 Data bit
7	0	Enable LSP1 Y_1 as GPIO

Table 1. Pass-Thru Bit Data Register

Absolute Maximum Ratings[NOTE(1)]

Supply Voltage(V_{CC}).....-0.3V to +4.0V
IDC Input Diode Current (I_{IK})
V_I = -0.5V.....-20 mA
DC Input Voltage (V_I).....0.5V to +3.9V
DC Output Diode Current (I_{OK})
V_o = -0.5V .....-20mA
DC Output Voltage (V_o).....-0.3V to +3.9V
DC Output Source /Sink Current (I_o).....±50mA
DC Vcc or Ground Current.....±50mA
per output Pin
DC Latchup Source or Sink Current .....±300mA
Junction Temperature (Plastic).....+150°C
Storage Temperature.....-65°C to +150°C

Lead Temperature (Solder, 5 sec)
100L BGA ..... 260°C
100L TQFP..... 260°C
Max Package Power Capacity @25°C
100L FBGA.....3.57W
100L TQFP.....2.11W
Thermal Resistance (θ_{JA})
100L FBGA.....35°C/W
100L TQFP.....59.1°C/W
Package Derating above +25°C
100L FBGA.....28.57mW/°C
100L TQFP.....16.92mW/°C
ESD Ratings
HBM[NOTE(1)].....4 KV
MM[NOTE(2)].....250V
CDM[NOTE(3)].....1.25 KV

NOTE(1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE(1) Human Body Model, applicable standard JESD22-A114-C
NOTE(2) Machine Model, applicable standard JESD22-A115-A
NOTE(3) Field Induced Charge Device Model, applicable standard JESD22-C101-C

Recommended Operating Conditions

Symbol	Parameter	Pins	MIN	TYP	MAX	Unit
V_{CC}	Supply Voltage	V_{CC}	3.0		3.6	V
V_I	Input Voltage	V_I	0		V_{CC}	V
V_o	Output Voltage	V_o	0		V_{CC}	V
T_A	Operating Temperature	All	-40		85	°C

DC Electrical Characteristics

Over recommended operating supply voltage and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{IH}	Minimum high input voltage		2.0			V
V_{IL}	Maximum Low input voltage				0.8	V
V_{oH}	Minimum high output voltage All outputs and I/O pins	I_{out}=-100 µA $V_{IN} = V_{IH}$ or V_{IL}	VCC - 0.2V			V
V_{oH}	Minimum high output voltage TDO_{BO}, TDO_{B1}, $TRIST_{BO}$, $TRIST_{B1}$, YO_{BO}, $Y1_{BO}$, YO_{B1}, $Y1_{B1}$, $TDO_{(01-06)}$, YO_{01}, $Y1_{01}$, $TRIST_{(01-03)}$	I_{out} = -12 mA All outputs loaded	2.4			V
V_{oH}	Minimum high output voltage TMS_{BO}, TMS_{B1}, TCK_{BO}, TCK_{B1}, $TRST^*_{BO}$, $TRST^*_{B1}$, $TMS_{(01-06)}$ $TCK_{(01-06)}$, $TRST^*_{(01-06)}$,	I_{out} = -24 mA	2.2			V
V_{OL}	Maximum low output voltage All outputs and I/O pins	I_{out} = +100 µA $V_{IN} = V_{IH}$ or V_{IL}			0.2	V
V_{OL}	Maximum low output voltage TDO_{BO}, TDO_{B1}, $TRIST_{BO}$, $TRIST_{B1}$, YO_{BO}, $Y1_{BO}$, YO_{B1}, $Y1_{B1}$, $TDO_{(01-06)}$, YO_{01}, $Y1_{01}$, $TRIST_{(01-03)}$	I_{out} = +12 mA			0.4	
V_{OL}	Maximum low output voltage TMS_{BO}, TMS_{B1}, TCK_{BO}, TCK_{B1}, $TRST^*_{BO}$, $TRST^*_{B1}$, $TMS_{(01-06)}$ $TCK_{(01-06)}$, $TRST^*_{(01-06)}$,	I_{out} = +24 mA			0.55	
V_{IKL}	Maximum input clamp diode voltage	IIK = -18 mA			-1.2	V
I_{IN}	Maximum input leakage current (non-resistor input pins)	$V_{IN} = V_{CC}$ or GND			±5.0	µA
I_{ILR}	Input current Low (input and I/O pins with pull-up resistors: TDI_{B1}, TDI_{B0}, TMS_{BO}, TMS_{B1}, $TRST^*_{B0}$, $TRST^*_{B1}$, AO_{BO}, $A1_{BO}$, AO_{B1}, $A1_{B1}$, $TDI_{(01-06)}$, AO_{01}, $A1_{01}$)	V_{IN} = GND	-25		-200	µA
I_{IH}	Input High Current (Input and I/O pins with pull-up resistors: TDI_{B1}, TDI_{B0}, TMS_{BO}, TMS_{B1}, $TRST^*_{B0}$, $TRST^*_{B1}$, AO_{BO}, $A1_{BO}$, AO_{B1}, $A1_{B1}$, $TDI_{(01-06)}$, AO_{01}, $A1_{01}$)	$V_{IN} = V_{CC}$			5.0	µA
I_{OFF}	Power-off Leakage Current Outputs and I/O pins without pull-up resistors	V_{CC} = 0V, V_{IN} = 3.6V (Note 3)			±5.0	µA
I_{OZ}	Maximum TRI-STATE Leakage Current Outputs and I/0 pins without pull-up resistors				±5.0	µA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND			3.8	mA
I_{CCD}	Maximum Dynamic Supply Current	$V_{IN} = V_{CC}$ or GND, Input, Freq = 25MH_Z			68	mA

AC Electrical Characteristics: Scan Bridge Mode

Over recommended operating supply voltage and temperature ranges unless otherwise specified.
RL = 500Ω to GND, CL = 50pf to GND, TR/TF = 2.5ns, Vmeasure = VCC/2

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
tPHL, tPLH	Progpagation Delay TCK_{B0} to TDO_{BO} or TDO_{B1}			8.5		ns
tPHL, tPLH	Propagation Delay TCK_{B1} to TDO_{BO} or TDO_{B1}			8.5		ns
tPHL tPLH	Propagation Delay TCK_{B0} to $TDO_{(01-06)}$			7.5		ns
tPHL tPLH	Propagation Delay TCK_{B1} to $TDO_{(01-06)}$			7.5		ns
tPHL tPLH	Propagation Delay TMS_{B0} to TMS_{B1}			8.0		ns
tPHL tPLH	Propagation Delay TMS_{B1} to TMS_{B0}			8.0		ns
tPHL tPLH	Propagation Delay TMS_{B0} to $TMS_{(01--6)}$			8.0		ns
tPHL tPLH	Propagation Delay TMS_{B1} to $TMS_{(01--6)}$			8.0		ns
tPHL tPLH	Propagation Delay TCK_{B0} to TCK_{B1}			8.0		ns
tPHL tPLH	Propagation Delay TCK_{B1} to TCK_{B0}			8.0		ns
tPHL tPLH	Propagation Delay TCK_{B0} to $TCK_{(01-06)}$			7.5		ns
tPHL tPLH	Propagation Delay TCK_{B1} to $TCK_{(01-06)}$			7.5		ns
tPHL tPLH	Propagation Delay TCK_{B0} to $TRST^*_{B1}$			11.5		ns
tPHL tPLH	Propagation Delay TCK_{B1} to $TRST^*_{B0}$			11.5		ns
tPHL tPLH	Propagation Delay TCK_{B0} to $TRST^*_{(01-06)}$			12.0		ns

AC Electrical Characteristics: Scan Bridge Mode (Continued)

Over recommended operating supply voltage and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
tPHL	Propagation Delay TCK_{Bn} to $TRIST_{BN}$			8.5		ns
tPHL	Propagation Delay TCK_{Bn} to $TRIST_{(01-03}$			8.0		ns
tPZL tPZH	Propagation Delay TCK_{Bn} to $TDO_{(01-06)}$ or $TDO_{(01-06)}$			9.0		ns
tPHL tPLH	Propagation Delay An to Yn			6.0		ns

AC Timing Characteristics: Scan Bridge Mode

Over recommended operating supply voltage and temperature ranges unless otherwise specified.
RL = 500Ω to GND, CL = 50pf to GND, TR/TF = 2.5ns, Vmeasure = VCC/2

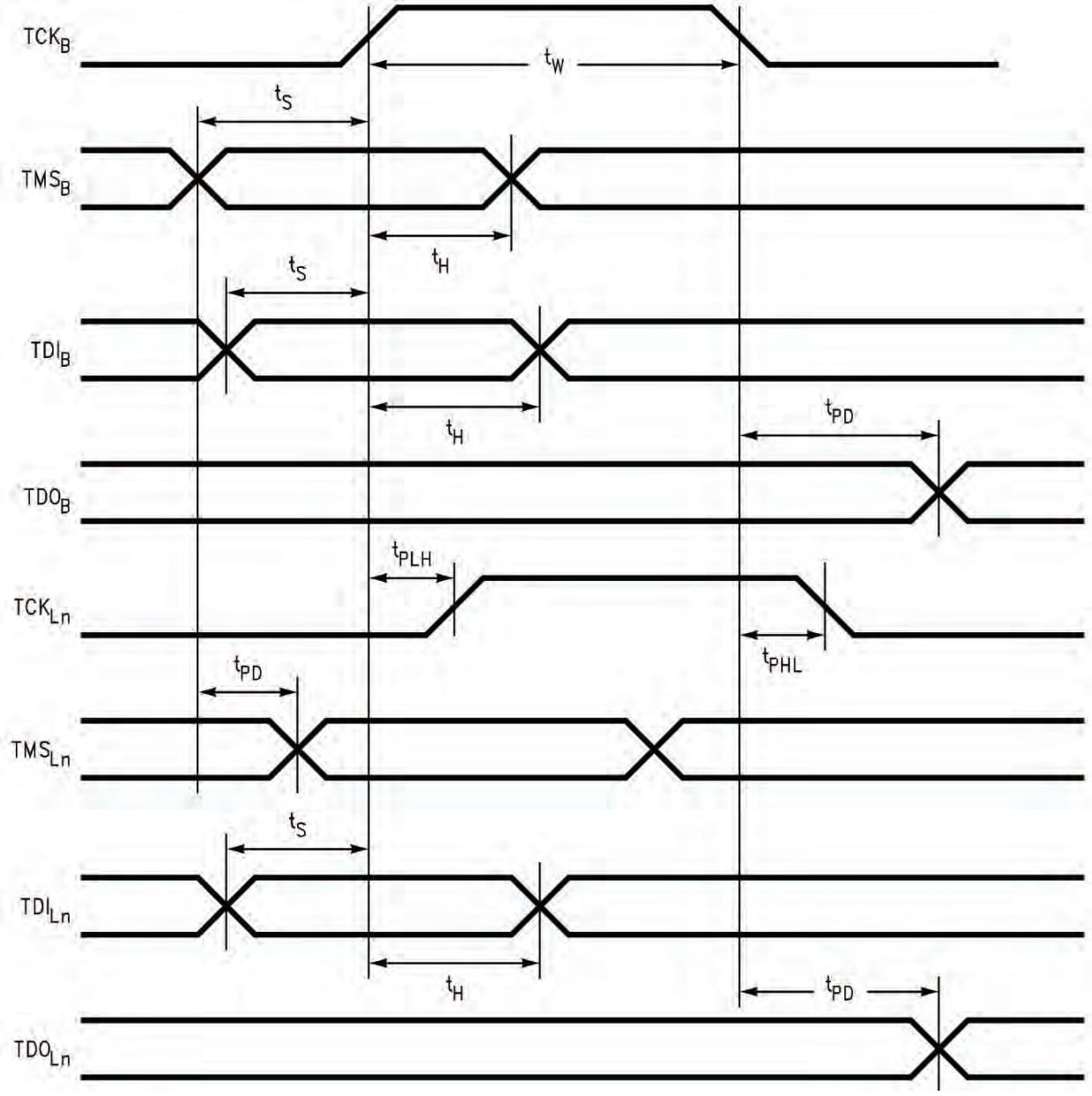
Symbol	Parameter	Conditions	TYP	Unit
t_s	Setup time TMS_{Bn} to TCK_{Bn}		2.5	ns
t_H	Hold Time TMS_{Bn} to TCK_{Bn}		1.5	ns
t_s	Setup Time TDI_{Bn} to TCK_{Bn}		3.0	ns
t_H	Hold Time TDI_{Bn} to TCK_{Bn}		2.0	ns
t_S	Setup Time $TDI_{(01-06)}$ to TCK_{Bn}		1.0	ns
t_H	Hold Time $TDI_{(01-06)}$ to TCK_{Bn}		3.5	ns
t_{REC}	Recovery Time TCK_{Bn} from $TRST_{Bn}$		1.0	ns
t_w	Clock Pulse Width TCK_{Bn}(H or L)	tR/tF = 1.0ns	10.0	ns
t_WL	Reset Pulse Width $TRST^*_{Bn}$(L)	tR/tF = 1.0ns	2.5	ns
F_{MAX}	Maximum Clock Frequency (Note 6)	tR/tF = 1.0ns	25	ns

AC Electrical Characteristics: Stitcher Mode

Over recommended operating supply voltage and temperature ranges unless otherwise specified.

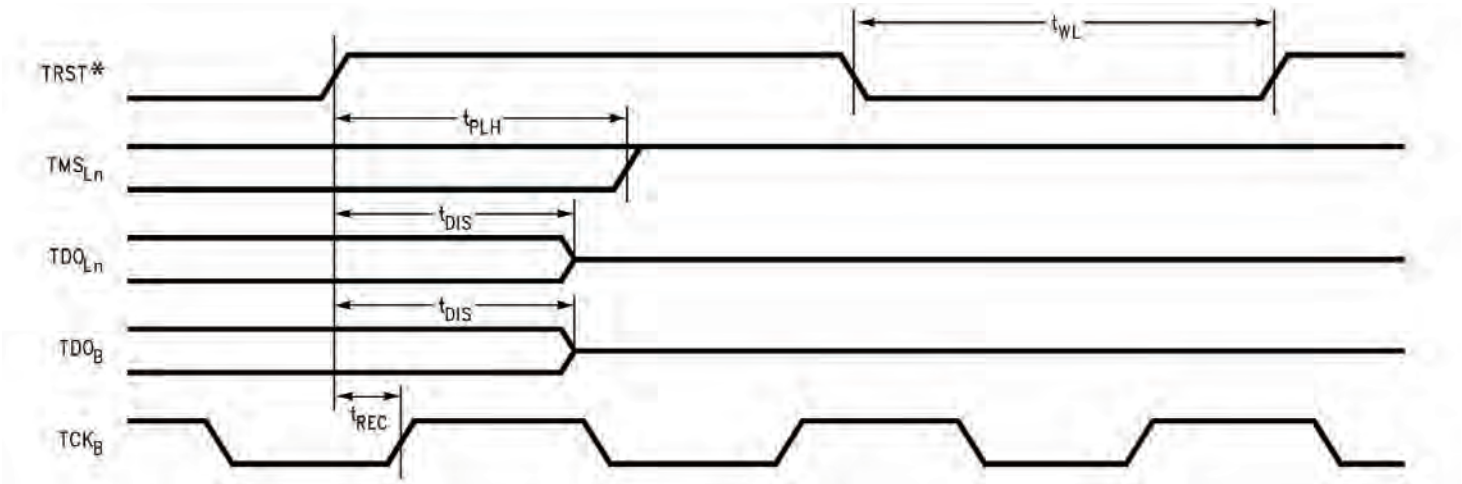
Parameter	Conditions	TYP	Units
tPHL, tPLH	Propagation Delay TDI_{B0} to $TDO_{B1,}$ TDI_{B1} to TDO_{B0}	12.5	ns
tPHL, tPLH	Propagation Delay TDI_{B0} to $TDO_{01,}$ TDI_{B1} to TDO_{01}	12.5	ns
tPHL, tPLH	Propagation Delay TDI_{LSPn} to TDO_{LSPn+1}	12.5	ns
tPHL, tPLH	Propagation Delay TMS_{B0} to $TMS_{B1,}$ TMS_{B1} to TMS_{B0}	12.5	ns
tPHL, tPLH	Propagation Delay TMS_{B0} to $TMS_{(01-06),}$ TMS_{B1} to $TMS_{(01-06)}$	12.5	ns
tPHL, tPLH	Propagation Delay $TRST^{\bullet}_{B0}$ to $TRST^{\bullet}_{B1,}$ $TRST^{\bullet}_{B1}$ to $TRST^{\bullet}_{B0}$	12.5	ns
tPHL, tPLH	Propagation Delay $TRST^{\bullet}_{B0}$ to $TRST^{\bullet}_{(01-06),}$ $TRST^{\bullet}_{B1}$ to $TRST^{\bullet}_{(01-06)}$	12.5	ns

Timing Diagrams

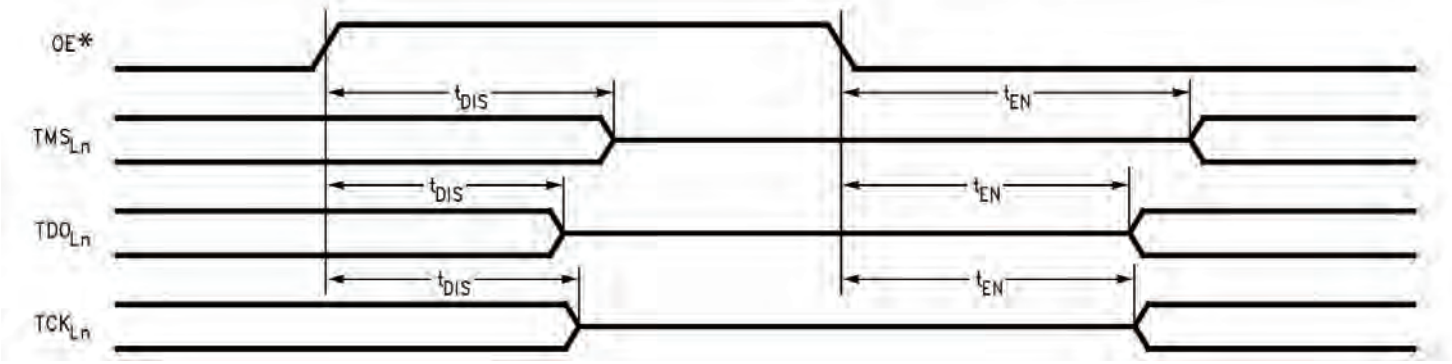


ScanBridge mode Waveforms

Timing Diagrams

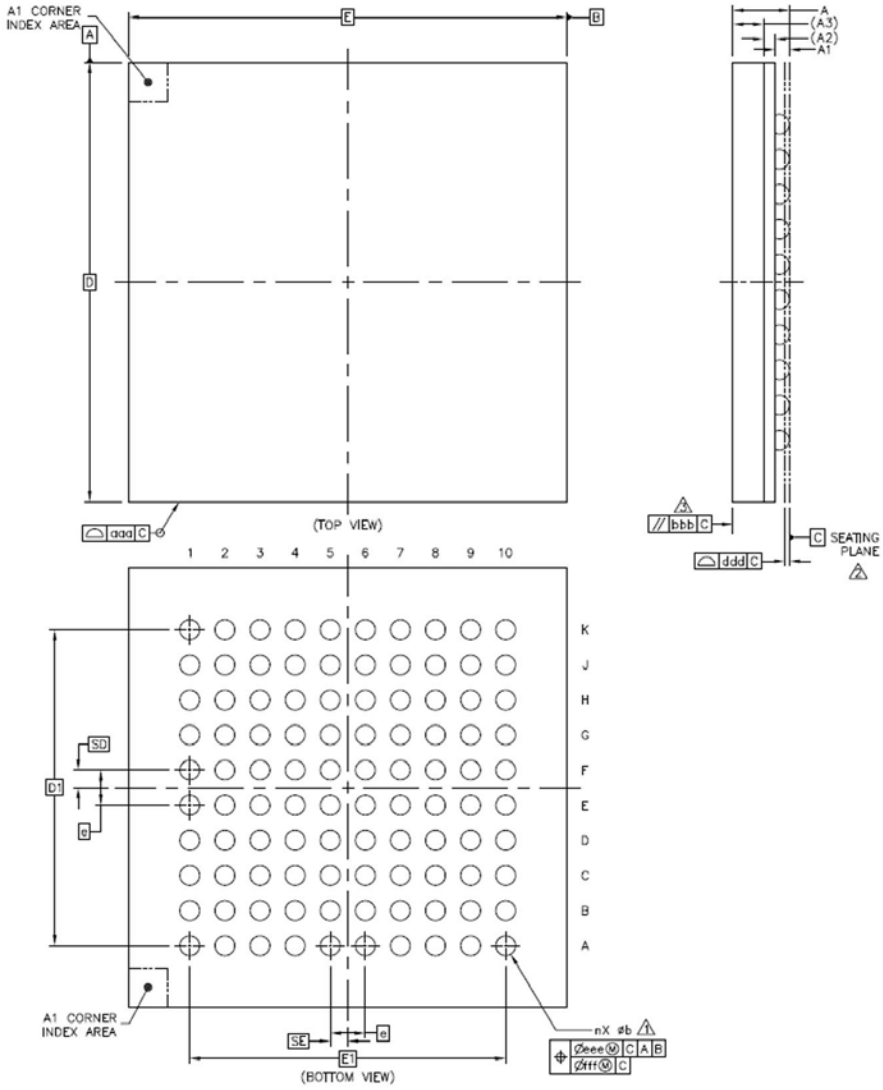


Reset Waveforms



Output Enable Waveforms

BGA-100 Package Dimensions



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1.4
STAND OFF	A1	0.25	---	0.4
SUBSTRATE THICKNESS	A2		0.26	REF
MOLD THICKNESS	A3		0.7	REF
BODY SIZE	D		10	BSC
	E		10	BSC
BALL DIAMETER			0.45	
BALL OPENING			0.4	
BALL WIDTH	b	0.4	---	0.5
BALL PITCH	e		0.8	BSC
BALL COUNT	n		100	
EDGE BALL CENTER TO CENTER	D1		7.2	BSC
	E1		7.2	BSC
BODY CENTER TO CONTACT BALL	SD		0.4	BSC
	SE		0.4	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.1	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

NOTES:

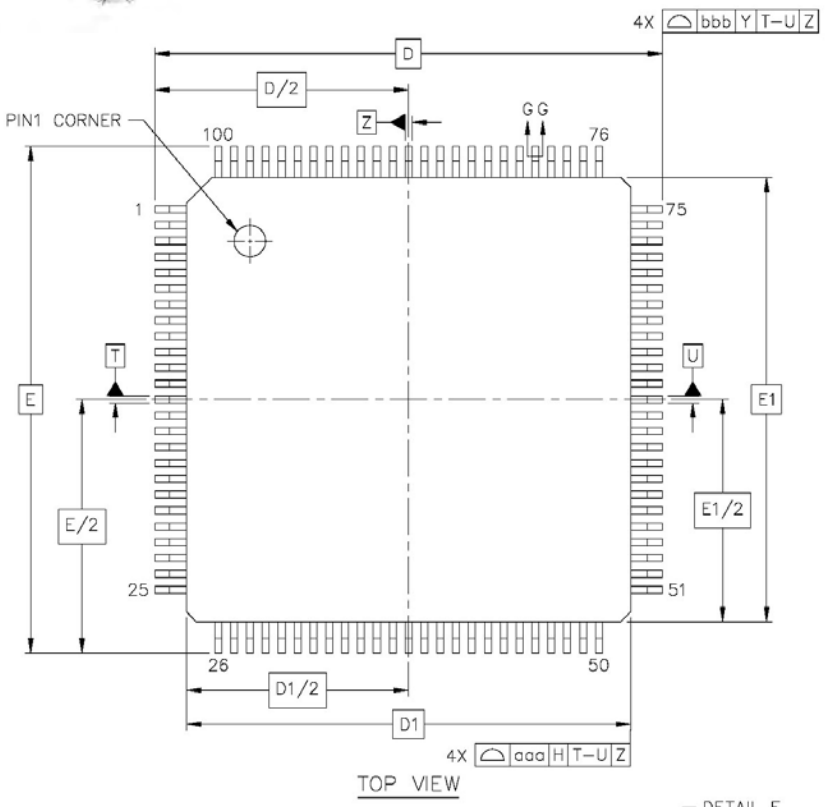
1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

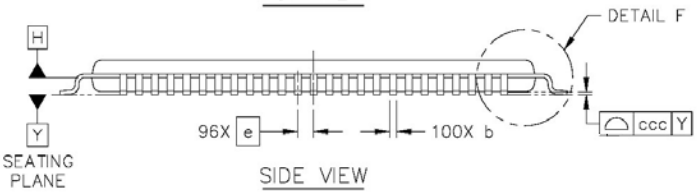
TITLE	DWG. NO.	REV.
PACKAGE OUTLINE 100 BALLS LFBGA 10 X 10 X 1.4 MM 0.8 PITCH	98A0100MB045	A01
	SHEET	SIZE
		A4

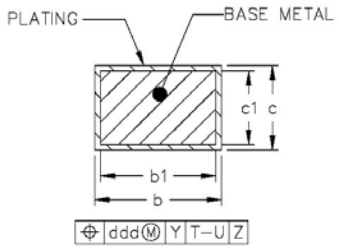
UNIT	DIMENSION AND TOLERANCES	REFERENCE DOCUMENT
MM	Y14.5M	---

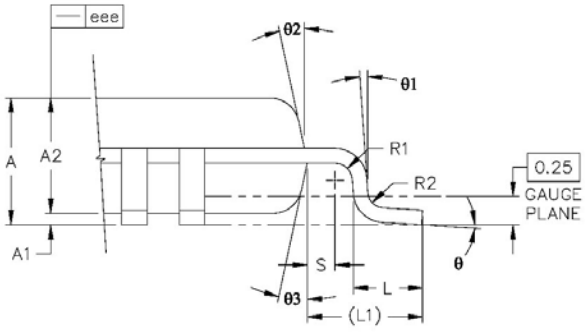
BGA-100

TQFP-100 Package Dimensions









NOTES

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. DIMENSIONS D1 AND E1 ARE MAXIMUN PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07MM FOR 0.4MM AND 0.5MM PITCH PACKAGES.

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.2
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	0.95	---	1.05
LEAD WIDTH(PLATING)		b	0.17	0.22	0.27
LEAD WIDTH		b1	0.17	0.2	0.23
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	16 BSC		
	Y	E	16 BSC		
	X	D1	14 BSC		
	Y	E1	14 BSC		
LEAD PITCH		e	0.5 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.08		
MOLD FLATNESS		eee	0.05		

Notes

Important Notice

For additional information please contact support@telefunkensemi.com or visit www.telefunkensemiconductors.com