TELEFUNKEN
Semiconductors

ADVANCE INFO

TF1125/1123/1121

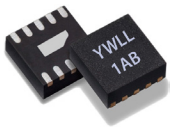
200V High Speed Logic Level MOSFET Gate Driver

Features:

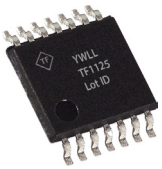
- **Floating high-side driver in bootstrap operation to 200V**
- **1.2A/5A (TF1125), 0.8A/3.3A (TF1123), 0.4/1.67A (TF1121) peak source/sink current**
- **0.4Ω/2Ω pull down/pull up impedance**
- **Independent high-side and low-side logic inputs**
- **High speed gate drivers at 5V supply**
- **Proprietary bootstrap capacitor auto-recharge technology**
- **Fast propagation delays (25ns typical)**
- **Separate source and sink outputs**

Applications

- High Speed DC-DC Converters
- High frequency Power Supplies
- Wireless Charging



TDFN-10



eTSSOP-14

Description

The TF1125/1123/1121 are high-side/low-side gate drivers with 5V supply giving the ability to drive logic level MOSFETs. The high-side driver features a floating supply for operation to 200V.

The three parts, TF1125/1123/1121, differ by output source/sink current (1.2A/5A, 0.8A/3.3A, 0.4A/1.67A respectively). For all the devices, a high sink capability maintains the gate drive line at a low level during high dv/dt prohibiting unintended turn on of the MOSFET.

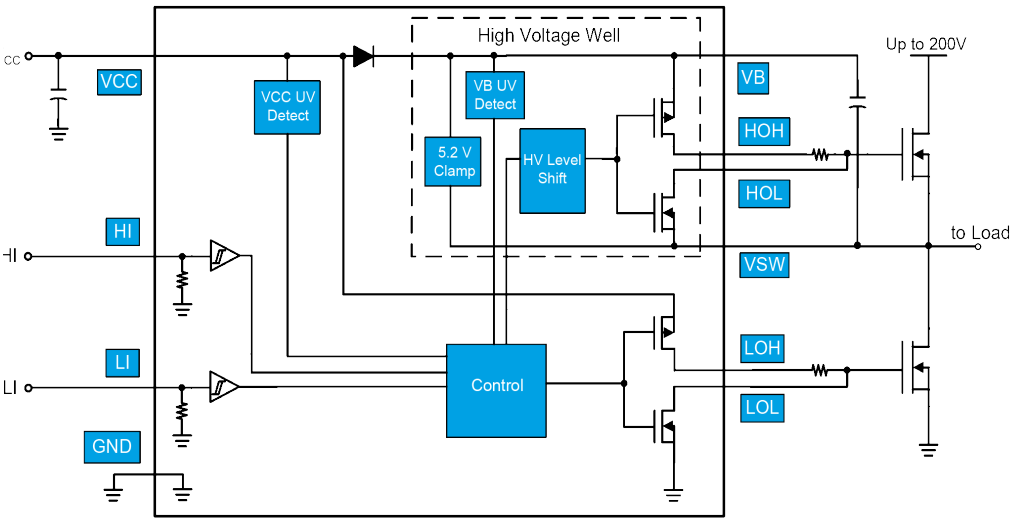
Ultra fast propagation delays and rise/fall times with a proprietary bootstrap capacitor auto-recharge allow high frequency operation with smaller component footprints; and with the integrated bootstrap diode, and the small TDFN-10 and TSSOP-14 package, the required area compared to a discrete solution is greatly reduced.

Ordering Information

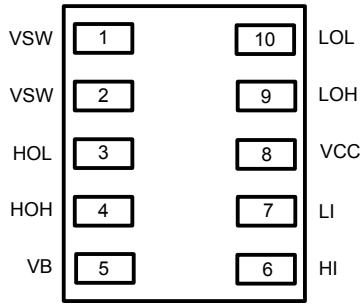
Year Week LLot ID

PART NUMBER	PACKAGE	PACKING / Qty	MARK
TF1125/1123/1121-NBP	TDFN-10	T & R / 3,000	YWLL PART#
TF1125/1123/1121-6BG	eTSSOP-14	T & R / 1,000	YWLL TF11XX Lot ID

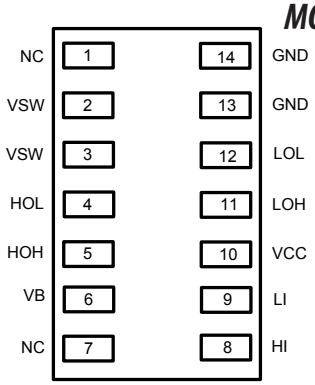
Typical Application



Pin Diagrams



Top View: TDFN-10



Top View: eTSSOP-14

TF1125/1123/1121

Pin Descriptions

PIN NAME	PIN DESCRIPTION
VSW	High-side bootstrap return
HOL	High-side gate driver sink output
HOH	High-side gate driver source output
VB	High-side bootstrap supply
HI	High-side gate driver control input
LI	Low-side gate driver control input
VCC	Low-side gate driver supply and control supply
LOH	Low-side gate driver source output
LOL	Low-side gate driver sink output
GND	Low-side and control ground, PAD for both packages

Absolute Maximum Ratings *(NOTE1)*

V_B - High side floating supply voltage.....-0.3V to +207V
V_S - High side floating supply offset voltage.....V_B-7V to V_B+0.3V
V_{HO} - High side floating output voltage.....V_S-0.3V to V_B+0.3V
dV_S / dt - Offset supply voltage transient.....50 V/ns

V_{CC} - Logic & low side fixed supply voltage.....-0.3V to +7V
V_{LO} - Low side output voltage.....-0.3V to V_{CC}+0.3V

V_{IN} - Logic input voltage (HI and LI).....-0.3V to +7V

P_D - Package power dissipation at $T_A \leq 25$ °C
TDFN-10.....TBD
eTSSOP-14.....TBD

NOTE1 *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

TDFN-10 Thermal Resistance ***(NOTE2)***
θ_{JA}.....TBD °C/W
eTSSOP-14 Thermal Resistance ***(NOTE2)***
θ_{JA}.....TBD °C/W

T_J - Junction operating temperature .....-40 °C to +150 °C
T_L - Lead temperature (soldering, 10s) ..... +300 °C
T_{stg} - Storage temperature range .....-55 °C to +150 °C

NOTE2 *When mounted on a standard JEDEC 2-layer FR-4 board.*

Recommended Operating Conditions (NOTE3)

Symbol	Parameter	MIN	MAX	Unit
V_B	High side floating supply absolute voltage	V_S + 4	V_S + 5.5	V
V_S	High side floating supply offset voltage	-5	200	V
V_{HO}	High side floating output voltage	V_S	V_B	V
V_{CC}	Low side fixed supply voltage	4.5	5.5	V
V_{LO}	Low side output voltage	0	V_{CC}	V
V_{IN}	Logic input voltage (HI & LI)	0	5	V
T_A	Ambient temperature	-40	125	°C

NOTE3 *Voltage amplitudes referenced to GND.*

DC Electrical Characteristics

V_{CC}=V_{BS} = 5V, T_A = 25°C and V_{SW} = GND = 0V, and no load on LOL, LOH, HOL, and HOH, unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{CC}	Supply Voltage		4.5	5.0	5.5	V
V_{IH}	Logic "1" input voltage		3.8			
V_{IL}	Logic "0" input voltage				1.2	
I_{CCQ}	Quiescent V_{CC} supply current	LI = HI = 0V		50		µA
I_{CCO}	Operating V_{CC} supply current	f = 500kHz		0.5		mA
I_{BSQ}	Quiescent V_{BS} supply current	LI = HI = 0V		80		µA
I_{BSO}	Operating V_{BS} supply current	f = 500kHz		1.0		mA
I_{IHYS}	Input Hysteresis			2.5		
V_{CCUV+}	V_{CC} supply under-voltage positive going threshold			3.7		V
V_{CCUV-}	V_{CC} supply under-voltage negative going threshold			3.5		
V_{BSUV+}	V_{BS} supply under-voltage positive going threshold			3.7		
V_{BSUV-}	V_{BS} supply under-voltage negative going threshold			3.5		
$V_{BSClamp}$	Bootstrap supply clamp		4.7	5.2	5.5	
V_{DL}	Bootstrap diode low-current forward voltage	I_{VCC-VB} = 100µA		0.6		
V_{DH}	Bootstrap diode hi-current forward voltage	I_{VCC-VB} = 100mA		0.9		
V_{DB}	Bootstrap diode breakdown voltage		200			
V_{OH}	High-Level Output Voltage	I_{OH}=100mA		0.2		
V_{OL}	Low-Level Output Voltage	I_{OL}=100mA		0.06		
I_{OH}	Peak source current	TF1125		1.2		A
		TF1123		0.8		
		TF1121		0.4		
I_{OL}	Peak sink current	TF1125		5.0		A
		TF1123		3.3		
		TF1121		1.67		
I_{OHLK}	High-level output leakage current	HOH = LOH = 0V		1.5		µA
I_{OLLK}	Low-level output leakage current	HOL = LOL = 5V		1.5		µA

AC Electrical Characteristics

$V_{CC} = V_{BS} = 5V$, $T_A = 25$ °C and V_{SW} = GND = 0V, and no load on LOL, LOH, HOL, and HOH, unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
t_{ONL}	LO turn-on propagation delay	LI rising to LOH rising		25		ns
t_{OFFL}	LO turn-off propagation delay	LI falling to LOL falling		25		
t_{ONH}	HO turn-on propagation delay	HI rising to HOH rising		25		
t_{OFFH}	HO turn-off propagation delay	HI falling to HOL falling		25		
$t_{DM\ ON}$	Delay Matching: LO on & HO off			1.5		
$t_{DM\ OFF}$	Delay Matching: LO off & HO on			1.5		
t_{HR}	HO rise time (0.5V - 4.5V)	CL = 1000pF		7.0		
t_{LR}	LO rise time (0.5V - 4.5V)	CL = 1000pF		7.0		
t_{HF}	HO fall time (0.5V - 4.5V)	CL = 1000pF		1.5		
t_{LF}	LO fall time (0.5V - 4.5V)	CL = 1000pF		1.5		
t_{PW}	Minimum input pulse width that changes the output			10		
t_{BS}	Bootstrap diode reverse recovery time			40		

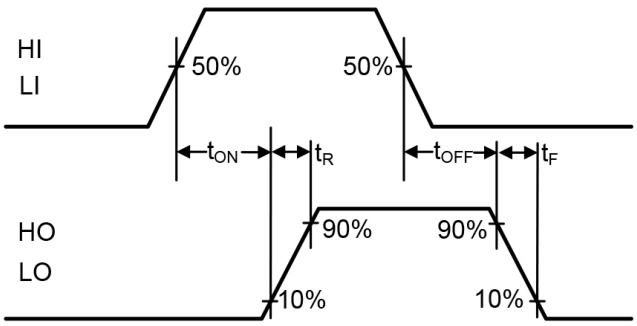


Figure 1. Switching Time Waveform Definitions

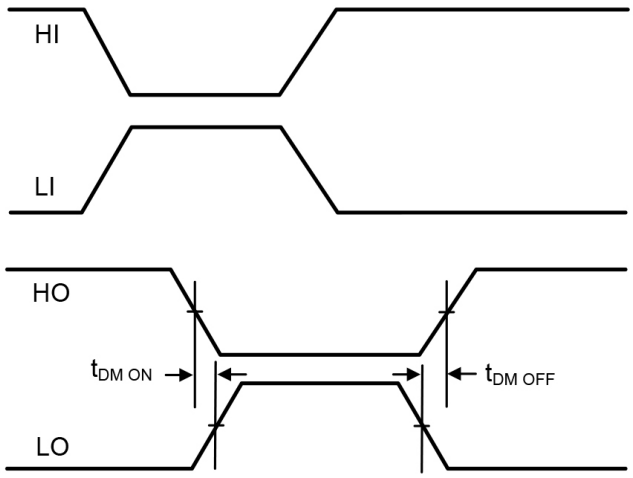
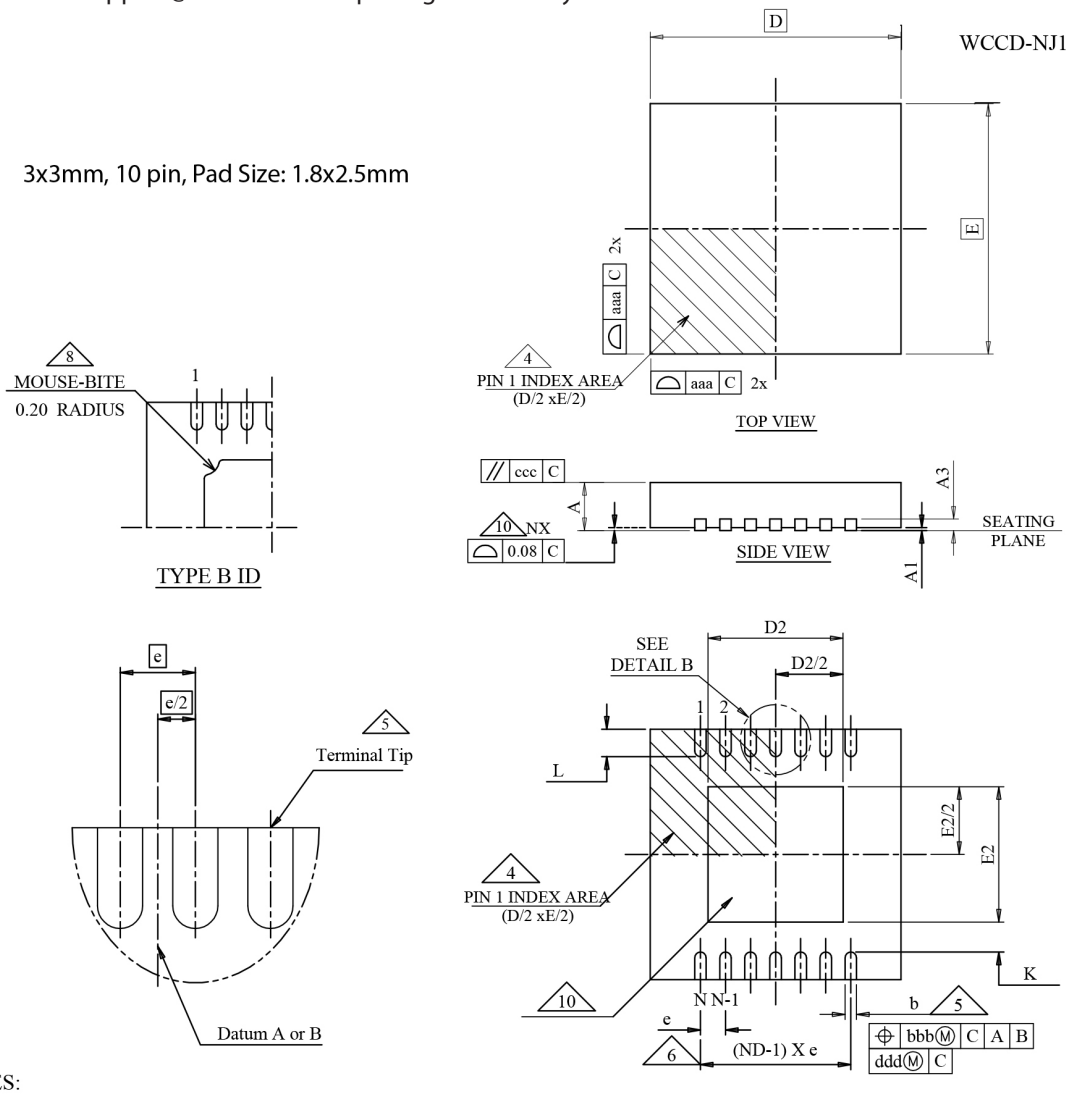


Figure 2. Delay Matching Waveform Definitions

Package Dimensions (TDFN-10)

Please contact support@tfsemi.com for package availability.

3x3mm, 10 pin, Pad Size: 1.8x2.5mm



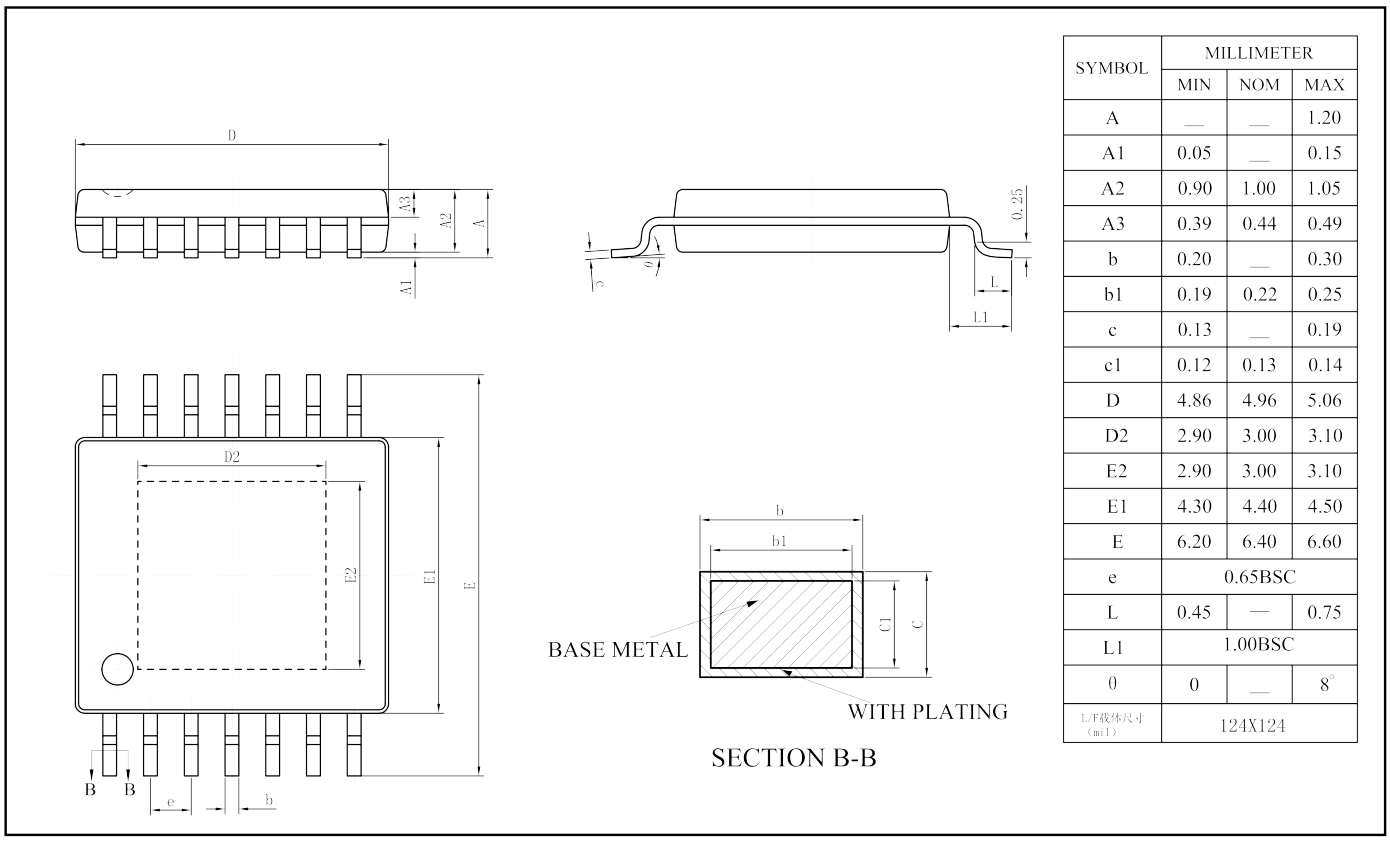
NOTES:

1. Dimensions in table are the TF4601, WCCD-NJ1 variation of the MLP Dual Family Package Outline.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. All dimensions are in millimeters, angle is in degrees (°).
4. N is the total number of terminals.
5. The terminal #1 identifier and terminal numbering convention shall conform to JESD 95-1 SPP-012. Details of terminal #1 identifier are optional, but must be located within the zone indicated. The terminal #1 identifier may be either a mold, embeded metal or mark feature.
6. Dimension b applies to metallized terminal and is measured between 0.15MM and 0.30MM from terminal tip.
7. ND refers to the maximum number of terminals on D side.
8. For a complete set of dimensions for each variation, see the individual variation and the common dimensions and tolerances on page 4.
9. Unilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.
10. In the case of the rectangular package, the terminal side of the package is determined as followed:
    a) Type 1: The terminals are on the short side of the package.
    b) Type 2: The terminals are on the long side of the package.
11. Variation codes reference specific JEDEC MO-229 package variations. However, codes starting with NJR are not currently JEDEC registered and not defined in the 'Variation Designation' table. Variation with a star (*) symbol are also not JEDEC registered.
12. When more than one variation (option) exists for the same profile height, body size (DxE), and pitch then those variations will be denoted by an additional dash number (i.e. -1,-2, etc) designator to identify them. The new variations would be created from all or any of the following reasons : Terminal count, Terminal length and/or exposed pad sizes.
13. Variation with Exposed Tie Bars do not comply with JEDEC OUTLINE MO-229

Dimension		MIN	NOM	MAX
A	Height	0.70	0.75	0.80
D	Length		2.0	
E	Width		2.0	
A1		0.00	0.02	0.05
A3			0.20 Ref	
e	Pitch		0.50	
K			0.20	
b	Lead Width	0.18	0.25	0.30
D2	DAP Length	1.55	1.70	1.80
E2	DAP Height	0.75	0.90	1.00
L		0.20	0.30	0.40

Package Dimensions (eTSSOP-14)

Please contact support@tfsemi.com for package availability.



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.30
b1	0.19	0.22	0.25
c	0.13	—	0.19
c1	0.12	0.13	0.14
D	4.86	4.96	5.06
D2	2.90	3.00	3.10
E2	2.90	3.00	3.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	—	0.75
L1	1.00BSC		
θ	0	—	8°
L/F载体尺寸 (mil)	124X124		

Notes

Important Notice

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