TELEFUNKEN
Semiconductors

Advance Info

TF2190(4)

High-Side and Low-Side Gate Driver

Features

- **Floating high-side driver in bootstrap operation to 600V**
- **Drives two N-channel MOSFETs or IGBTs in a half-bridge configuration**
- **Output drivers capable of 4.5A/4.5A typ sink/source**
- **Logic input (HIN and LIN) 3.3V capability**
- **Schmitt triggered logic inputs with internal pulldown**
- **Undervoltage lockout for high and low-side drivers**
- **Extended temperature range: -40°C to +125°C**

Description

The TF2190 is a high voltage, high speed gate driver capable of driving N-channel MOSFET's and IGBTs in a half-bridge configuration. TF Semi's high voltage process enables the TF2190's high side to switch to 600V in a bootstrap operation under high dV/dt conditions.

The TF2190 logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with controlling devices. The driver outputs feature high pulse current buffers designed for minimum driver cross conduction.

The TF2190 is offered in space saving 8-pin SOIC and the TF21904 in the 14-pin SOIC and operates over an extended -40°C to +125°C temperature range.

SOIC-8(N)

SOIC-14(N)

Applications

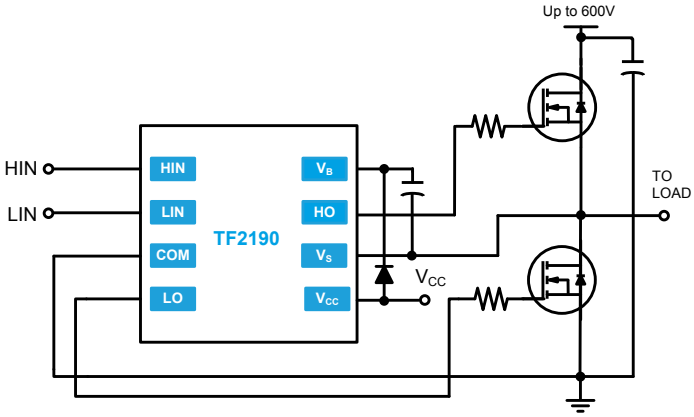
- Motor Controls
- DC-DC Converters
- AC-DC Inverters
- Class D Power Amplifiers

Ordering Information

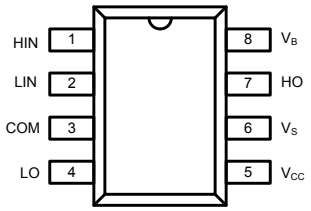
Year Year Week Week

PART NUMBER	PACKAGE	PACK / Qty	MARK
TF2190-TAH	SOIC-8(N)	T&R / 1500	TF YYWW TF2190 Lot ID
TF21904-TUH	SOIC-14(N)	T&R / 2500	TF YYWW TF21904 Lot ID

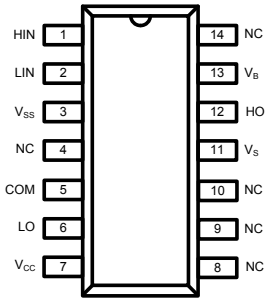
Typical Application



Pin Diagrams



Top View: SOIC-8(N), TF2190

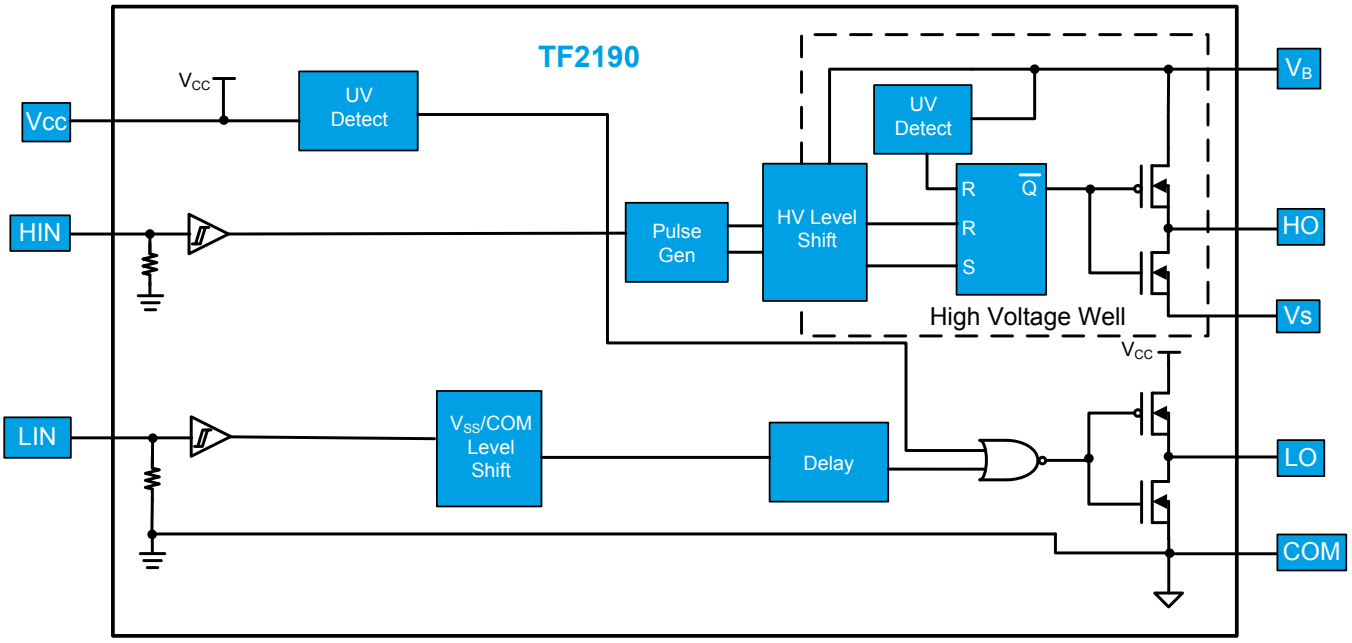


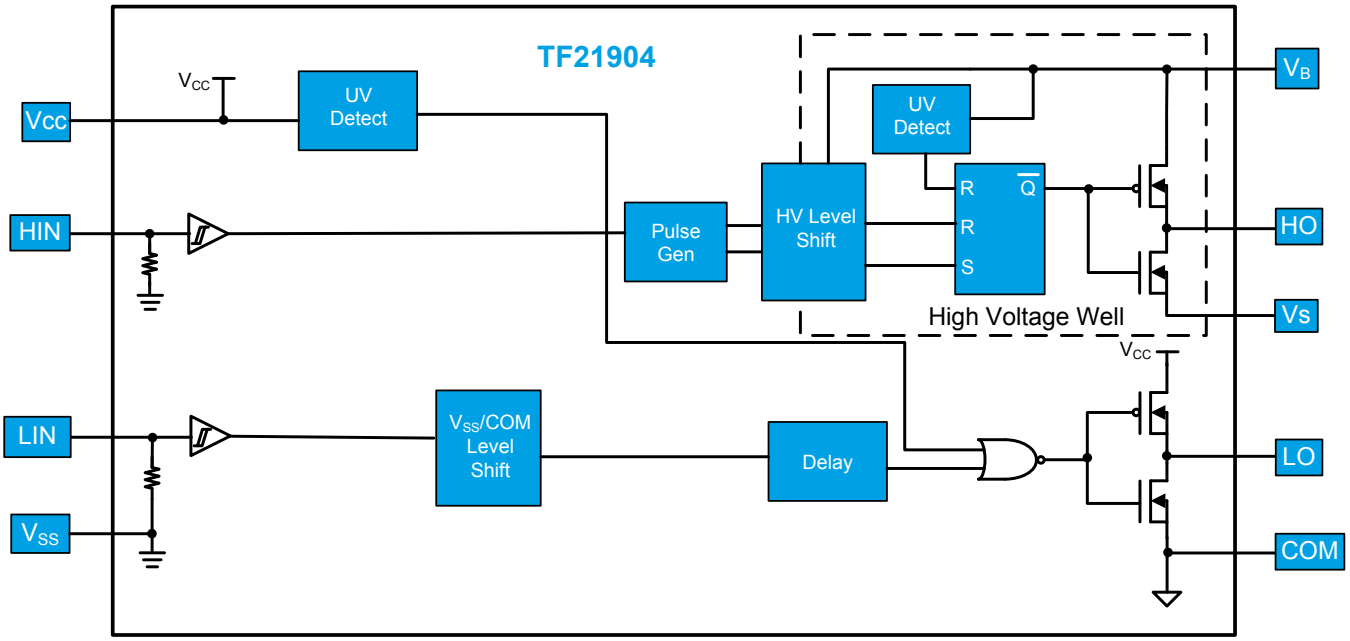
Top View: SOIC-14(N), TF21904

Pin Descriptions

PIN NAME	PIN DESCRIPTION
HIN	Logic input for high-side gate driver output, in phase with HO
LIN	Logic input for low-side gate driver output, in phase with LO
COM	Low-side and logic return
LO	Low-side gate drive output
V_{CC}	Low-side and logic fixed supply
V_S	High-side floating supply return
HO	High-side gate driver output
V_B	High-side floating supply
V_{SS}	Logic Ground (TF21904 only)

Functional Block Diagrams





Absolute Maximum Ratings *(NOTE1)*

V_B - High side floating supply voltage.....-0.3V to +624V
V_S - High side floating supply offset voltage....V_B-24V to V_B+0.3V
V_{SS} - Logic Supply offset voltage.....V_{CC} -24V to V_{CC} + 0.3V
V_{HO} - High side floating output voltage.....V_S-0.3V to V_B+0.3V
dV_S / dt - Offset supply voltage transient.....50 V/ns

V_{CC} - Low side and logic fixed supply voltage.....-0.3V to +24V
V_{LO} - Low side output voltage.....-0.3V to V_{CC}+0.3V
V_{IN} - Logic input voltage (HIN and LIN)... -0.3V to V_{CC}+0.3V

NOTE1 *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

P_D - Package power dissipation at $T_A \leq 25$ °C
SOIC-8.....0.625W
SOIC-14.....0.862W

SOIC-8 Thermal Resistance ***(NOTE2)***
θ_{JC}.....45 °C/W
θ_{JA}.....200 °C/W

SOIC-14 Thermal Resistance ***(NOTE2)***
θ_{JA}.....145 °C/W

T_J - Junction operating temperature .....+150 °C
T_L - Lead temperature (soldering, 10s) ..... +300 °C
T_{stg} - Storage temperature range .....-55 °C to +150 °C

NOTE2 *When mounted on a standard JEDEC 2-layer FR-4 board.*

Recommended Operating Conditions

Symbol	Parameter	MIN	MAX	Unit
V_B	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	***NOTE3***	600	
V_{SS}	Logic ground (TF21904 only)	-5	5	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (HIN and LIN)	0	V_{CC}	
T_A	Ambient temperature	-40	125	°C

NOTE3 *Logic operational for VS of -5V to +600V. Logic state held for VS of -5V to -VBS*

DC Electrical Characteristics *(NOTE4)*

V_{BIAS} (V_{CC}, V_{BS}) = 15V, T_A = 25 °C , unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{IH}	Logic "1" input voltage	V_{CC} = 10V to 20V	2.5			V
V_{IL}	Logic "0" input voltage				0.8	
V_{OH}	High level output voltage, V_{BIAS} - V_O	I_O = 0mA			0.1	
V_{OL}	Low level output voltage, V_O	I_O = 0mA			0.035	
I_{LK}	Offset supply leakage current	VB = VS = 600V			50	µA
I_{BSQ}	Quiescent V_{BS} supply current	V_{IN} = 0V or 5V		45	80	
I_{CCQ}	Quiescent V_{CC} supply current	V_{IN} = 0V or 5V		75	200	
I_{IN+}	Logic "1" input bias current	V_{IN} = 5V		25	50	
I_{IN-}	Logic "0" input bias current	V_{IN} = 0V		1.0	2.0	
V_{BSUV+}	V_{BS} supply under-voltage positive going threshold		7.6	8.4	9.8	V
V_{BSUV-}	V_{BS} supply under-voltage negative going threshold		6.9	7.8	9.0	
V_{CCUV+}	V_{CC} supply under-voltage positive going threshold		7.6	8.4	9.8	
V_{BSUV-}	V_{CC} supply under-voltage negative going threshold		6.9	7.8	9.0	
V_{CCUVH}	V_{CC} and V_{BS} under-voltage hysteresis			0.6		
V_{BSUVH}						
I_{O+}	Output high short circuit pulsed current	V_O = 0V, PW ≤ 10 ms	3.5	4.5		A
I_{O-}	Output low short circuit pulsed current	V_O = 15V, PW ≤ 10 ms	3.5	4.5		

NOTE4 *The V_{IN}, V_{TH}, and I_{IN} parameters are applicable to the two logic input pins: HIN and LIN. The V_0 and I_0 parameters are applicable to the respective output pins: HO and LO*

AC Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000pF, and T_A = 25 °C , unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
t_{on}	Turn-on propogation delay	V_S = 0V		140	200	ns
t_{off}	Turn-off propogation delay	V_S = 0V		140	200	
t_{DM}	Delay matching, HS & LS turn on/off			0	50	
t_r	Turn-on rise time	V_S = 0V		25	50	
t_f	Turn-off fall time			20	45	

Timing Waveforms

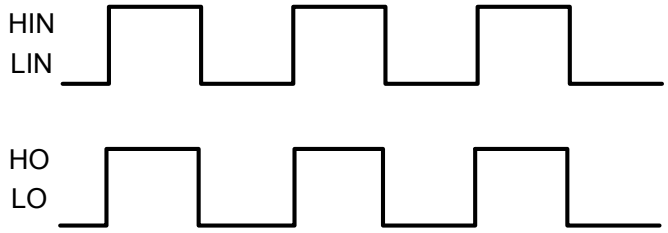


Figure 1. Input / Output Timing Diagram

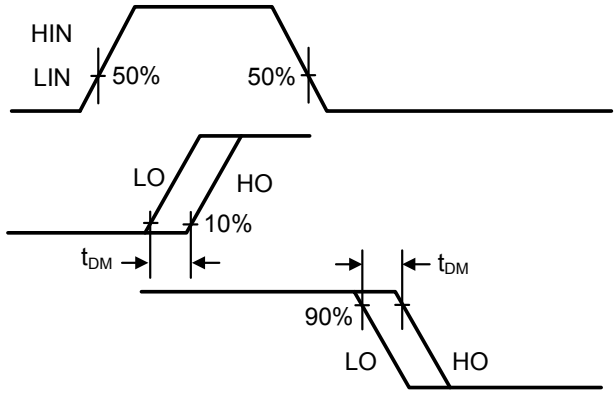


Figure 2. Delay Matching Waveform Definitions

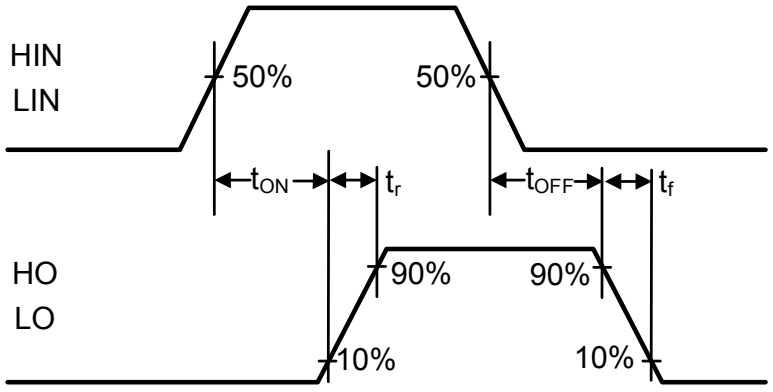
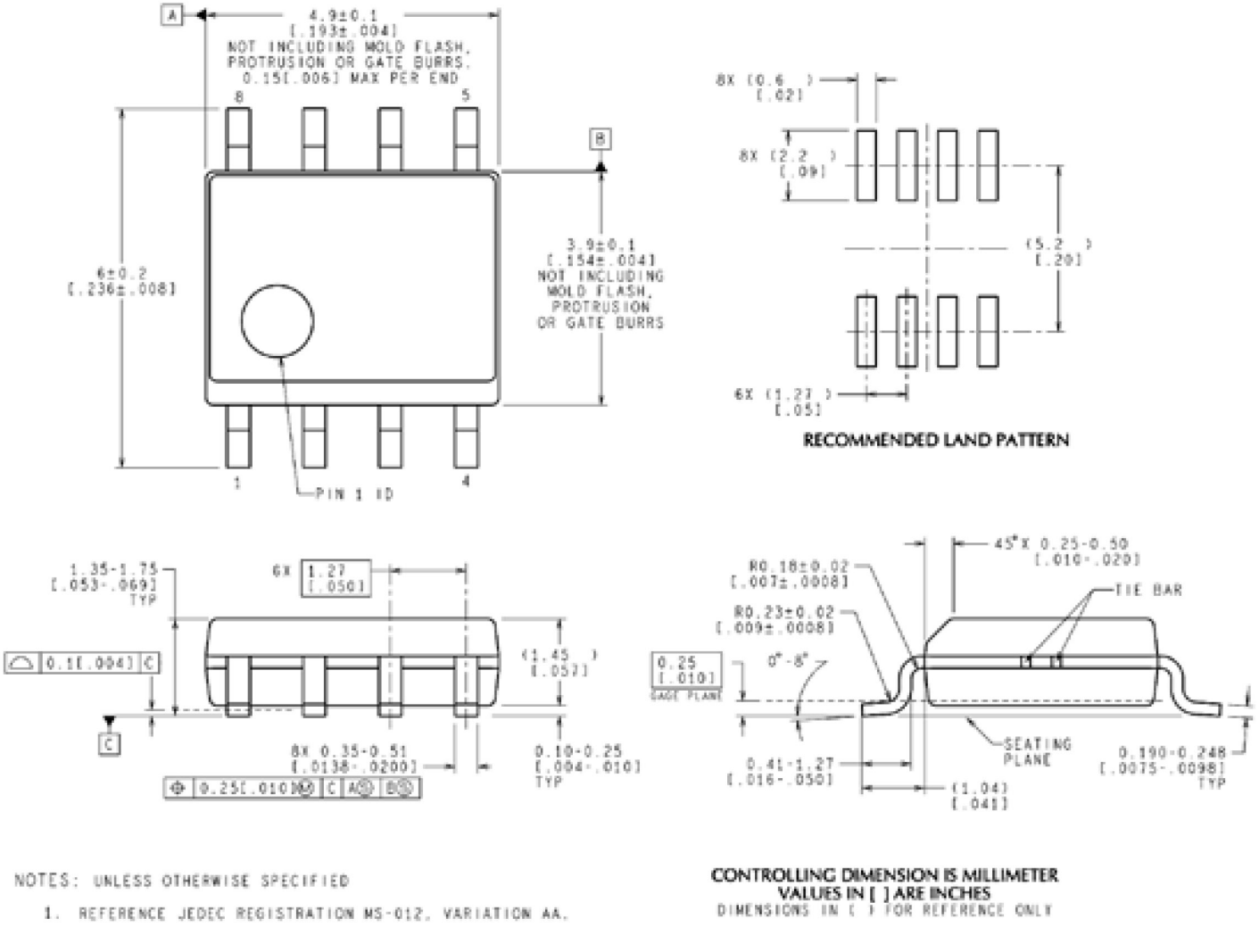


Figure 3. Switching Time Waveform Definitions

Package Dimensions (SOIC-8 N)

Please contact support@tfsemi.com for package availability.



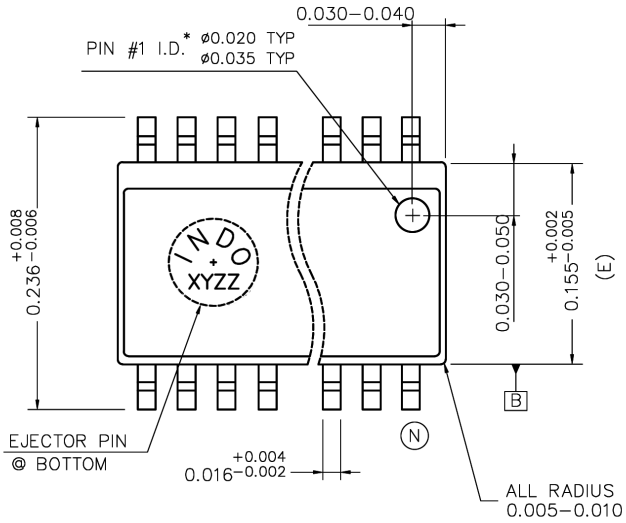
NOTES: UNLESS OTHERWISE SPECIFIED

1. REFERENCE JEDEC REGISTRATION MS-012, VARIATION AA.

CONTROLLING DIMENSION IS MILLIMETER
VALUES IN [ ] ARE INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

Package Dimensions (SOIC-14)

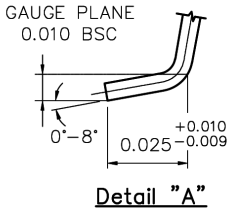
Please contact support@tfsemi.com for package availability.



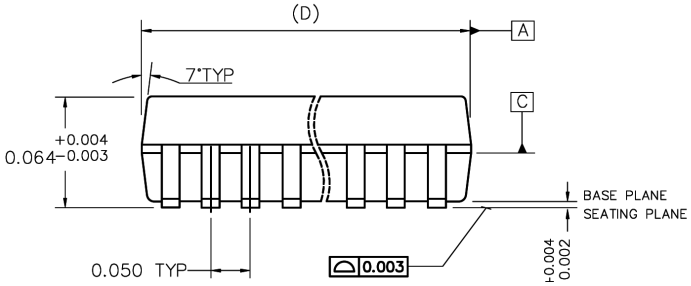
ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE NOTED

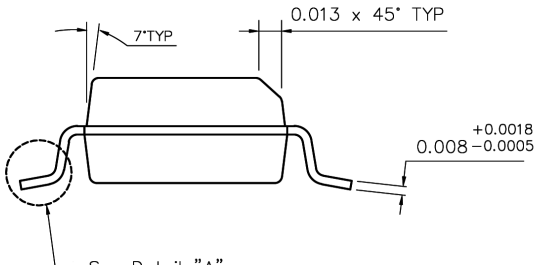
NOTES:

1. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSION. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 6 MILS PER SIDE.
2. "N" IS THE NUMBER OF TERMINAL POSITIONS.
3. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 3 MILS (⊕ SEATING PLANE) OUTGOING ASSEMBLY & 4 MILS AFTER TEST.
4. THE BOTTOM PACKAGE LEAD SIDE MAY BE BIGGER THAN THE TOP PACKAGE LEAD SIDE BY 4 MILS (2 MILS PER SIDE). BOTTOM PACKAGE DIMENSION SHALL FOLLOW DIMENSION STATED IN THIS DRAWING.
5. THE BOTTOM EJECTOR PIN CONTAINS COUNTRY OF ORIGIN "INDO" AND MOLD ID. (REFER TO TABLE FOR OPTION).
6. THIS DRAWING CONFORMS TO JEDEC REF. MS–012 REV. E



N	D VARIATION			MGP MOLD			
				STANDARD		MATRIX	
	MIN	NOM	MAX	PIN 1 I.D.	EJECT PIN	PIN 1 I.D.	EJECT PIN
08	0.189	0.193	0.196	N/A		YES	YES
14	0.337	0.339	0.344	YES	NO	YES	YES
⚠ 16	0.386	0.390	0.393	N/A		YES	YES





Notes

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