Advance Info

TF2184

Half-Bridge Gate Driver

TELEFUNKEN Semiconductors

Features

- **Floating high-side driver in bootstrap operation to 600V**
- **Drives two N-channel MOSFETs or IGBTs in a half bridge configuration**
- **1.4A source / 1.8A sink output current capability**
- **Outputs tolerant to negative transients**
- **Internal dead time of 400ns to protect MOSFETs**
- **Wide low side gate driver supply voltage: 10V to 20V**
- **Logic input (IN and SD*) 3.3V capability**
- **Schmitt triggered logic inputs with internal pull down**
- **Undervoltage lockout for high and low side drivers**
- **Extended temperature range: -40°C to +125°C**

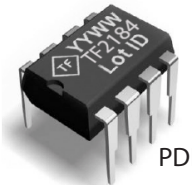
Description

The TF2184 is a high voltage, high speed gate driver capable of driving N-channel MOSFETs and IGBTs in a half bridge configuration. Telefunken's high voltage process enables the TF2184's high side to switch to 600V in a bootstrap operation.

The TF2184 logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with controlling devices. The driver outputs feature high pulse current buffers designed for minimum driver cross conduction. TF2184 has a fixed internal deadtime of 400ns (typical).

The TF2184 is offered in PDIP-8 and SOIC-8(N) packages and operate over an extended -40 °C to +125 °C temperature range.

SOIC-8(N)



PDIP-8

Applications

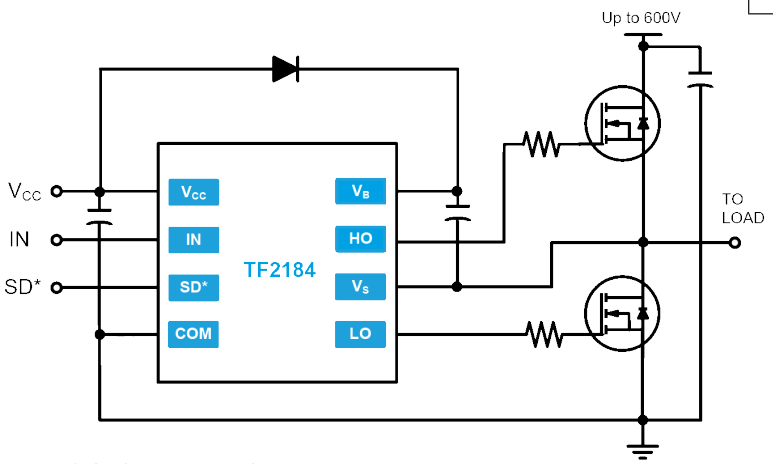
- DC-DC Converters
- AC-DC Inverters
- Motor Controls
- Class D Power Amplifiers

Ordering Information

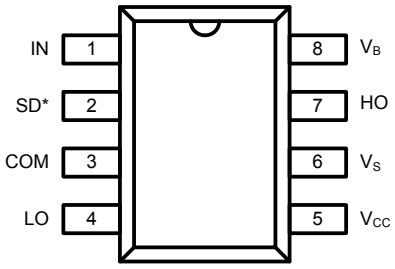
Year Year Week Week

PART NUMBER	PACKAGE	PACK / Qty	MARK
TF2184-3AS	PDIP-8	Tube / 50	TF YYWW TF2184 Lot ID
TF2184-TAU	SOIC-8(N)	Tube / 100	TF YYWW TF2184 Lot ID
TF2184-TAH	SOIC-8(N)	T&R / 2500	

Typical Application



Pin Diagrams



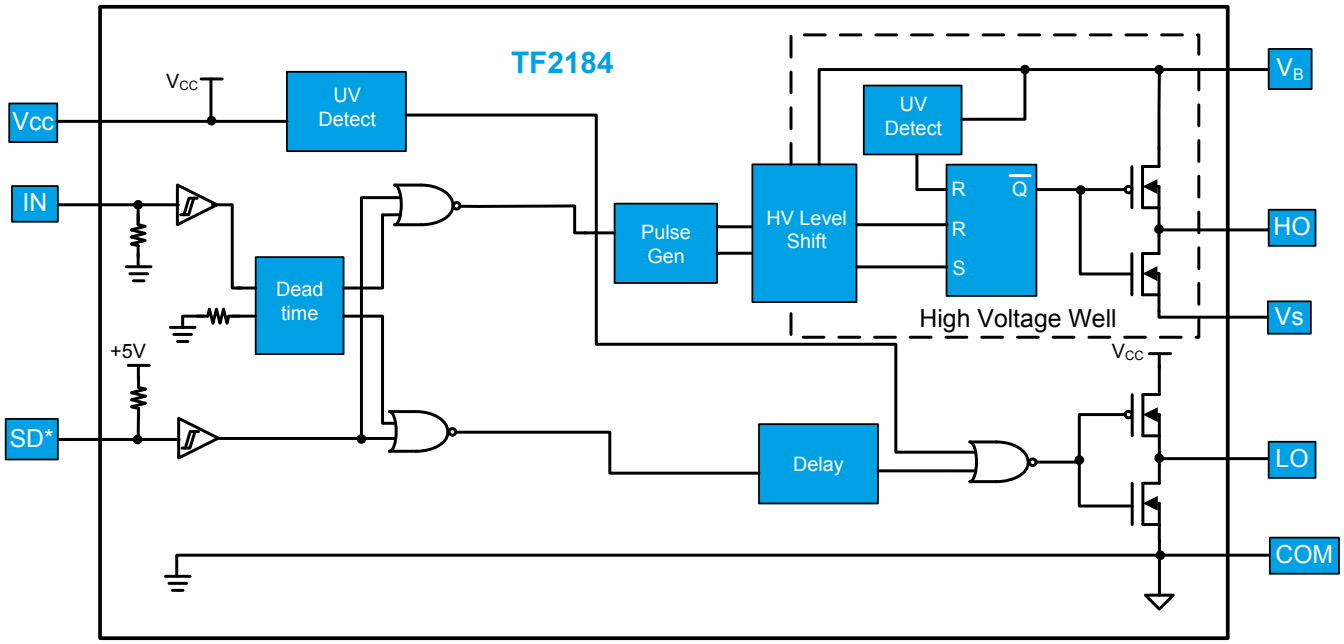
Top View: PDIP-8, SOIC-8

TF2184

Pin Descriptions

PIN NAME	PIN NUMBER	PIN DESCRIPTION
IN	1	Logic input for high-side and low-side gate driver outputs (HO and LO), in phase with HO.
SD*	2	Logic input for shutdown, enabled low
COM	3	Low-side and logic return
LO	4	Low-side gate drive output
V_{CC}	5	Low-side and logic fixed supply
V_S	6	High-side floating supply return
HO	7	High-side gate drive output
V_B	8	High-side floating supply

Functional Block Diagram



Absolute Maximum Ratings *(NOTE1)*

V_B - High side floating supply voltage.....-0.3V to +624V
V_S - High side floating supply offset voltage....V_B-24V to V_B+0.3V
V_{HO} - High side floating output voltage.....V_S-0.3V to V_B+0.3V
dV_S/dt - Offset supply voltage transient.....50 V/ns

V_{CC} - Low-side fixed supply voltage.....-0.3V to +24V
V_{LO} - Low-side output voltage.....-0.3V to V_{CC} +0.3V
V_{IN} - Logic input voltage (IN and SD*).....-0.3V to V_{CC} +0.3V

NOTE1 *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

P_D - Package power dissipation at $T_A \leq 25$ °C
SOIC-8.....0.625W
PDIP-8.....1.0W

SOIC-8(N) Thermal Resistance ***(NOTE2)***
θ_{JA}.....200 °C/W
PDIP-8 Thermal Resistance ***(NOTE2)***
θ_{JA}.....125 °C/W

T_J - Junction operating temperature.....+150 °C
T_L - Lead Temperature (soldering, 10 seconds).....+300 °C
T_{stg} - Storage temerature .....-55 to 150 °C

NOTE2 *Thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.*

Recommended Operating Conditions

Symbol	Parameter	MIN	MAX	Unit
V_B	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	***NOTE3***	600	V
V_{HO}	High side floating output voltage	V_S	V_B	V
V_{CC}	Low side fixed supply voltage	10	20	V
V_{LO}	Low side output voltage	0	V_{CC}	V
V_{IN}	Logic input voltage (IN and SD*)	0	V_{CC}	V
T_A	Ambient temperature	-40	125	°C

NOTE3 *Logic operational for VS of -5V to +600V. Logic state held for VS of -5V to -VBS*

DC Electrical Characteristics *(NOTE4)*

V_{BIAS} (V_{CC}, V_{BS}) = 15V, T_A = 25 °C , unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{IH}	Logic "1" input voltage	V_{CC} = 10V to 20V	2.5			V
V_{IL}	Logic "0" input voltage				0.8	
$V_{SD\ TH+}$	SD* input positive going threshold		2.5	50		
$V_{SD,\ TH-}$	SD* input negative going threshold			20	0.8	
V_{OH}	High level output voltage, V_{BIAS} - V_O	I_O = 0A			1.2	
V_{OL}	Low level output voltage, V_O	I_O = 20mA			0.1	
I_{LK}	Offset supply leakage current	VB = VS = 600V			50	µA
I_{BSQ}	Quiescent V_{BS} supply current	V_{IN} = 0V or 5V	20	60	150	
I_{CCQ}	Quiescent V_{CC} supply current	V_{IN} = 0V or 5V	0.4	1.0	1.8	mA
I_{IN+}	Logic "1" input bias current	IN = 5V, SD* = 0V		25	60	µA
I_{IN-}	Logic "0" input bias current	IN = 5V, SD* = 5V			1.0	
V_{BSUV+}	V_{BS} supply under-voltage positive going threshold		8.0	8.9	9.8	V
V_{BSUV-}	V_{BS} supply under-voltage negative going threshold		7.4	8.2	9.0	
V_{CCUV+}	V_{CC} supply under-voltage positive going threshold		8.0	8.9	9.8	
V_{CCUV-}	V_{CC} supply under-voltage negative going threshold		7.4	8.2	9.0	
I_{O+}	Output high short circuit pulsed current	V_O = 0V, PW ≤ 10 µs	1.4	1.9		A
I_{O-}	Output low short circuit pulsed current	V_O = 15V, PW ≤ 10 µs	1.7	2.3		

NOTE4 *The V_{IN}, V_{TH}, and I_{IN} parameters are applicable to the two logic input pins: IN and SD*. The V_0 and I_0 parameters are applicable to the respective output pins: HO and LO*

AC Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000pF, and T_A = 25 °C , unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
t_{on}	Turn-on propogation delay	V_S = 0V		680	900	ns
t_{off}	Turn-off propogation delay	V_S = 0V or 600V		270	400	
t_{SD}	Shut-down propogation delay			180	270	
$t_{DM\ ON}$	Delay matching, HS & LS turn-on				90	
$t_{DM\ OFF}$	Delay matching, HS & LS turn-off	I_O = 0A			40	
t_r	Turn-on rise time	V_S = 0V		40	60	
t_f	Turn-off fall time			20	35	
t_{DT}	Deadtime: $t_{DT\ LO\text{-}HO}$ & $t_{DT\ HO\text{-}LO}$		280	400	520	ns

Timing Waveforms

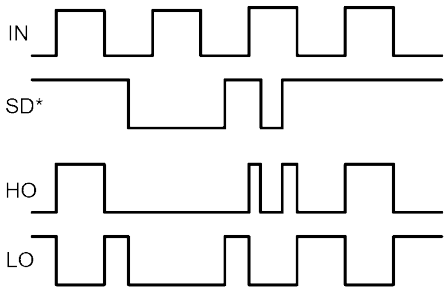


Figure 1. Input / Output Timing Diagram

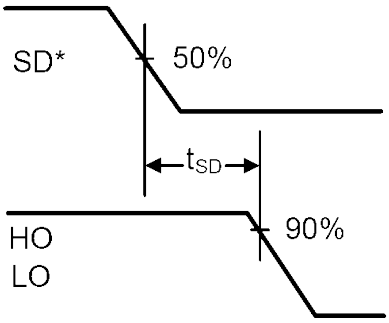
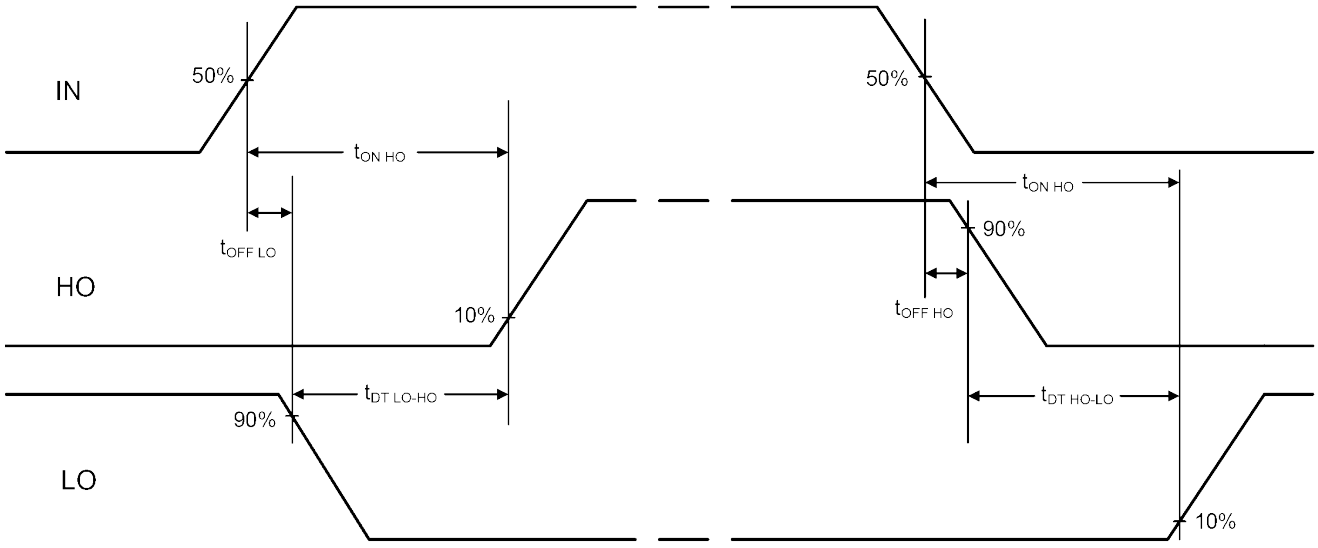


Figure 2. Shutdown Waveform Definitions



Deadtime $t_{DT\ LO-HO} = t_{ON\ HO} - t_{OFF\ LO}$
$t_{DT\ HO-LO} = t_{ON\ LO} - t_{OFF\ HO}$

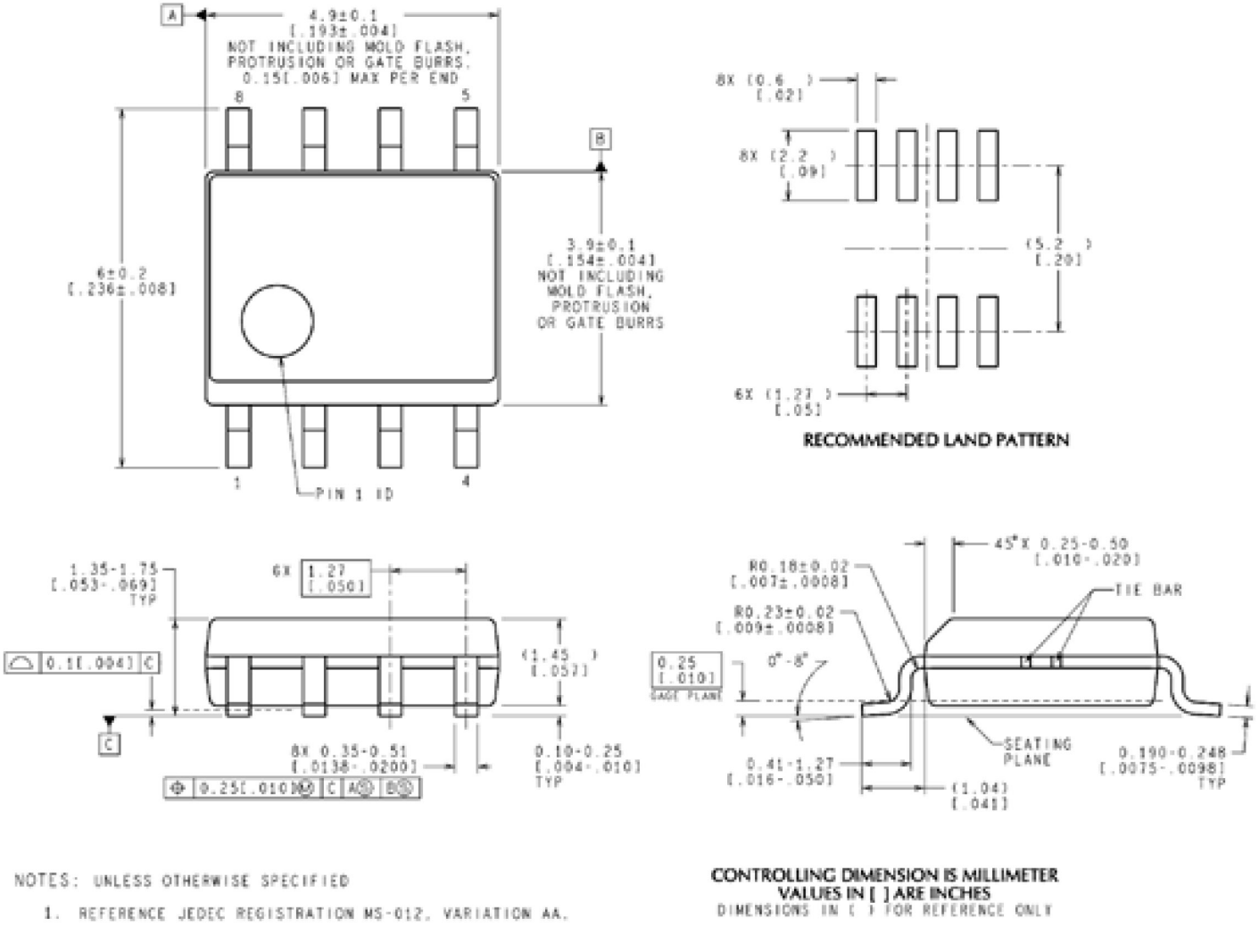
Deadtime matching
$t_{MDT} = t_{DT\ LO-HO} - t_{DT\ HO-LO}$

Delay matching
$t_{DM\ OFF} = t_{OFF\ LO} - t_{OFFT\ HO}$

Figure 3. Switching Time Waveform Definitions

Package Dimensions (SOIC-8 N)

Please contact support@tfsemi.com for package availability.



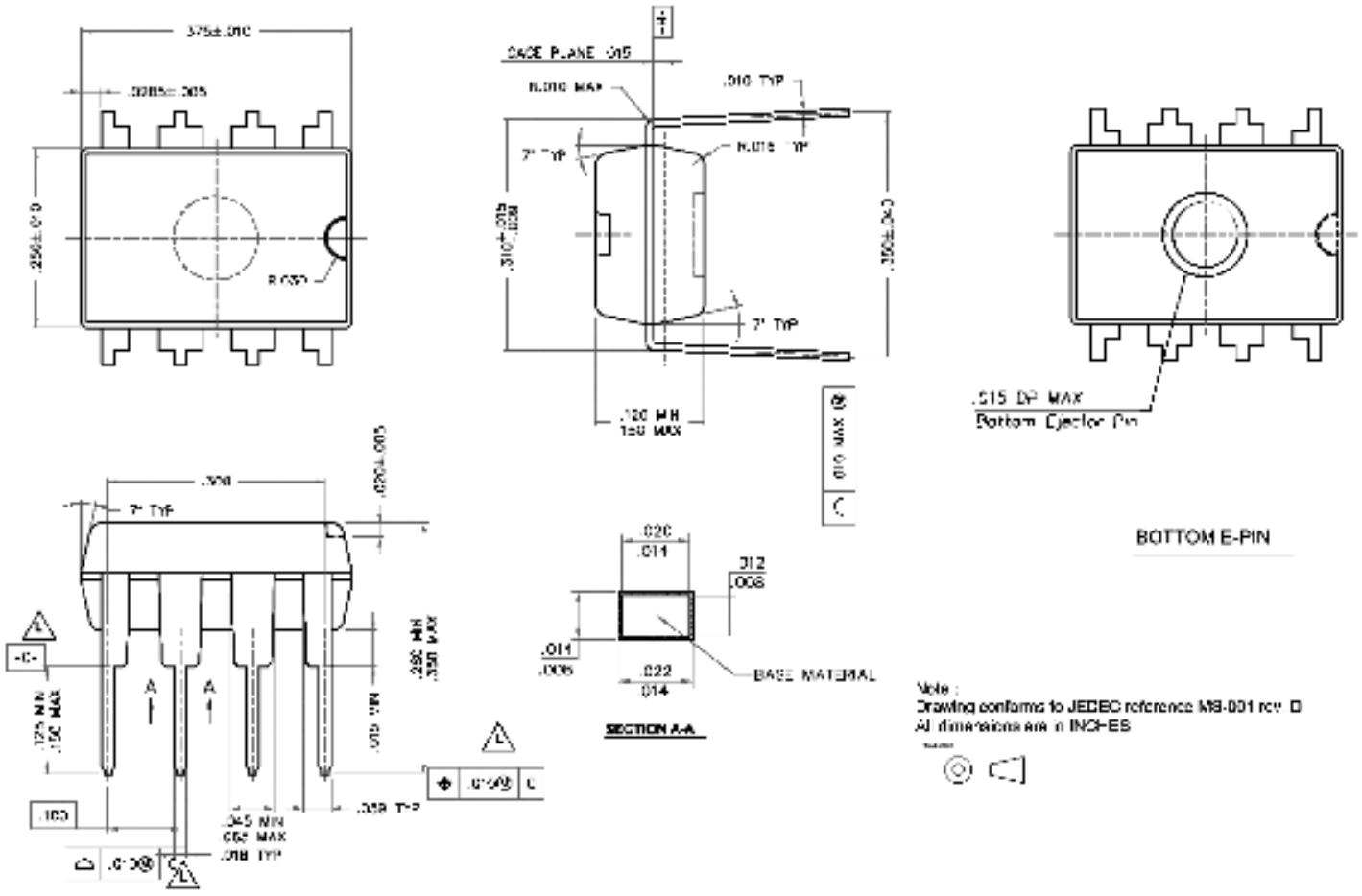
NOTES: UNLESS OTHERWISE SPECIFIED

1. REFERENCE JEDEC REGISTRATION MS-012, VARIATION AA.

CONTROLLING DIMENSION IS MILLIMETER
VALUES IN [ ] ARE INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

Package Dimensions (PDIP-8)

Please contact support@tfsemi.com for package availability.



Notes

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