TELEFUNKEN
Semiconductors

TF2101

High-Side and Low-Side Gate Driver

Features

- **Floating high-side driver in bootstrap operation to 600V**
- **Drives two N-channel MOSFETs or IGBTs in high-side/ low-side configuration**
- **Outputs tolerant to negative transients**
- **Wide low-side gate driver and logic supply: 10V to 20V**
- **Logic inputs CMOS and TTL compatible (down to 3.3V)**
- **Schmitt triggered logic inputs with internal pull down**
- **Undervoltage lockout for V_{CC}**
- **Space-saving SOIC-8 package available**
- **Extended temperature range:-40°C to +125°C**

Description

The TF2101 is a high voltage, high speed gate driver capable of driving N-channel MOSFETs and IGBTs in a high-side/low-side configuration. Telefunken's high voltage process enables the TF2101's high-side to switch to 600V in a bootstrap operation. The 50ns (max) propagation delay matching between the high and the low side drivers allows high frequency switching.

The TF2101 logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) for easy interfacing with controlling devices. The driver outputs feature high pulse current buffers designed for minimum driver cross conduction. The low-side gate driver and logic share a common ground

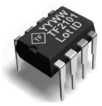
The TF2101 is available in a space-saving 8-pin SOIC package, an 8-pin PDIP, and a 14-pin SOIC package; the operating temperature extends from -40°C to +125°C .

Applications

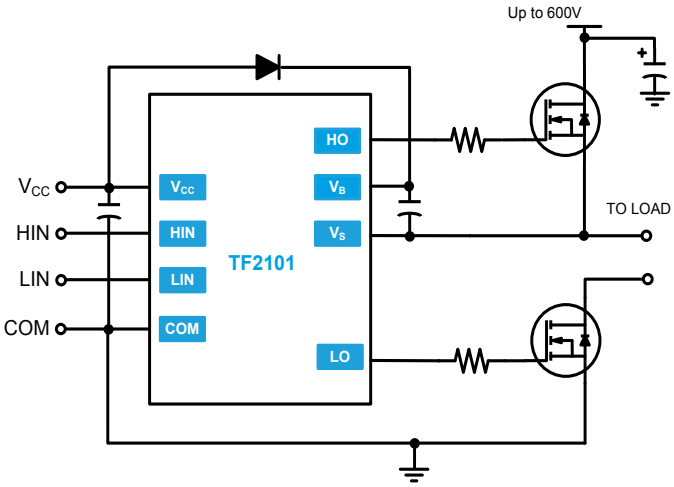
- DC-DC Converters
- AC-DC Inverters
- Motor Controls
- Class D Power Amplifiers


SOIC-8(N)


SOIC-14(N)


PDIP-8

Typical Application

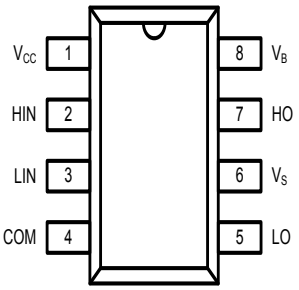


Ordering Information

Year Year Week Week

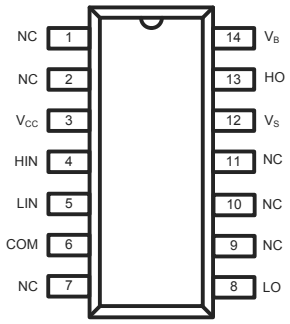
PART NUMBER	PACKAGE	PACK / Qty	MARK
TF2101-TAU	SOIC-8(N)	Tube / 100	YYWW TF2101 Lot ID
TF2101-TAH	SOIC-8(N)	T & R/ 2500	YYWW TF2101 Lot ID
TF2101-TUU	SOIC-14(N)	Tube / 50	YYWW TF2101 Lot ID
TF2101-TUH	SOIC-14(N)	T & R / 2500	YYWW TF2101 Lot ID
TF2101-3AS	PDIP-8	Tube / 50	YYWW TF2101 Lot ID

Pin Diagrams



Top View: PDIP-8, SOIC-8

TF2101



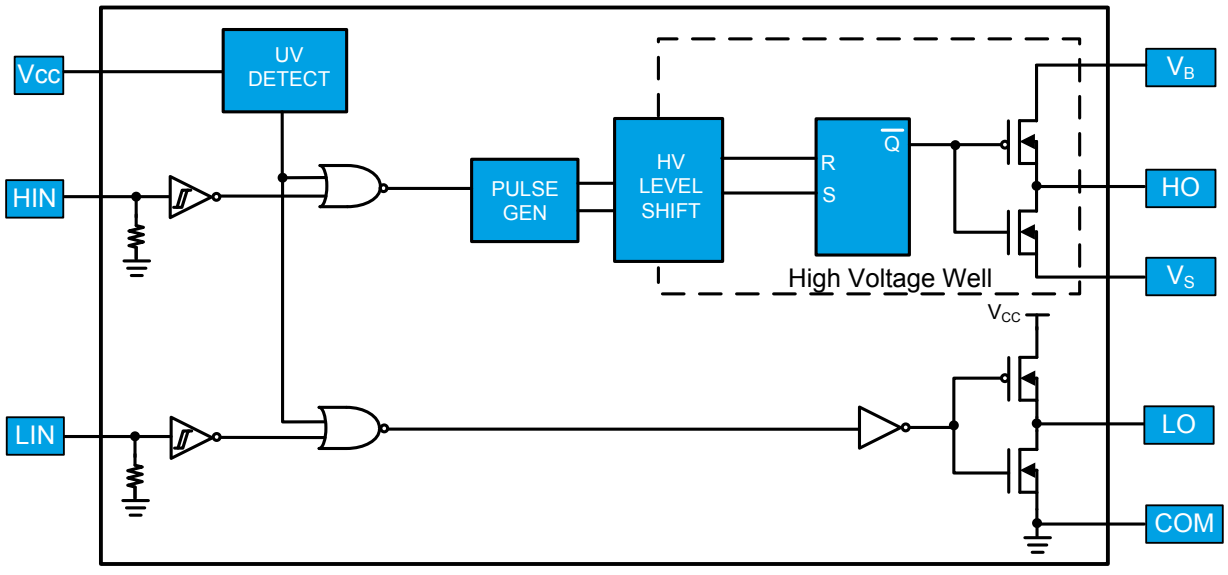
Top View: SOIC-14

TF2101

Pin Descriptions

PIN NAME	PIN DESCRIPTION
HIN	Logic input for high-side gate driver output (HO), in phase
LIN	Logic input for low-side gate driver output (LO), in phase
V_B	High-side floating supply
HO	High-side gate drive output
V_S	High-side floating supply return
V_{CC}	Low-side and logic fixed supply
LO	Low-side gate drive output
COM	Low-side return
NC	"No connect" pin

Functional Block Diagram



Absolute Maximum Ratings *(NOTE1)*

V_B - High side floating supply voltage.....-0.3V to +624V
V_S - High side floating supply offset voltage....V_B-24V to V_B+0.3V
V_{HO} - High side floating output voltage.....V_S-0.3V to V_B+0.3V
dV_S / dt - Offset supply voltage transient.....50 V/ns

V_{CC} - Low side and logic fixed supply voltage.....-0.3V to +24V
V_{LO} - Low side output voltage.....-0.3V to V_{CC}+0.3V
V_{IN} - Logic input voltage (HIN and LIN)... -0.3V to V_{CC}+0.3V

NOTE1 *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

P_D - Package power dissipation at $T_A \leq 25$ °C
SOIC-8.....0.625W
SOIC-14.....0.862W
PDIP-8.....1.0W

SOIC-8 Thermal Resistance ***(NOTE2)***
θ_{JC}.....45 °C/W
θ_{JA}.....200 °C/W

SOIC-14 Thermal Resistance ***(NOTE2)***
θ_{JA}.....145 °C/W

PDIP-8 Thermal Resistance ***(NOTE2)***
θ_{JC}.....35 °C/W
θ_{JA}.....125 °C/W

T_J - Junction operating temperature .....+150 °C
T_L - Lead temperature (soldering, 10s) ..... +300 °C
T_{stg} - Storage temperature range .....-55 °C to +150 °C

NOTE2 *When mounted on a standard JEDEC 2-layer FR-4 board.*

Recommended Operating Conditions

Symbol	Parameter	MIN	TYP	MAX	Unit
V_B	High side floating supply absolute voltage	V_S + 10		V_S + 20	V
V_S	High side floating supply offset voltage	***NOTE3***		600	V
V_{HO}	High side floating output voltage	V_S		V_B	V
V_{CC}	Low side and logic fixed supply voltage	10		20	V
V_{LO}	Low side output voltage	0		V_{CC}	V
V_{IN}	Logic input voltage (HIN and LIN)	COM		V_{CC}	V
T_A	Ambient temperature	-40		125	°C

NOTE3 *Logic operational for V_S = -5 to +600V.*

DC Electrical Characteristics *(NOTE4)*

V_{BIAS} (V_{CC}, V_{BS}) = 15V, T_A = 25 °C , unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{IH}	Logic "1" input voltage	V_{CC} = 10V to 20V	2.5			V
V_{IL}	Logic "0" input voltage	V_{CC} = 10V to 20V			0.8	V
V_{OH}	High level output voltage, V_{BIAS} - V_O	I_O = 2mA		0.05	0.2	V
V_{OL}	Low level output voltage, V_O	I_O = 2mA		0.02	0.1	V
I_{LK}	Offset supply leakage current	VB = VS = 600V			50	µA
I_{BSQ}	Quiescent V_{BS} supply current	V_{IN} = 0V or 5V		30	55	µA
I_{CCQ}	Quiescent V_{CC} supply current	V_{IN} = 0V or 5V		150	270	µA
I_{IN+}	Logic "1" input bias current	V_{IN} = 5V		3	10	µA
I_{IN-}	Logic "0" input bias current	V_{IN} = 0V			5	µA
V_{CCUV+}	V_{CC} supply under-voltage positive going threshold		8	8.9	9.8	V
V_{CCUV-}	V_{CC} supply under-voltage negative going threshold		7.4	8.2	9	V
I_{O+}	Output high short circuit pulsed current	V_O = 0V, V_{IN} = Logic "1", PW ≤ 10 µs	130	290		mA
I_{O-}	Output low short circuit pulsed current	V_O = 15V, V_{IN} = Logic "0", PW ≤ 10 µs	270	600		mA

AC Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, T_A = 25 °C, and C_L = 1000pF, unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
t_{ON}	Turn-on propagation delay	V_S = 0V		160	220	ns
t_{OFF}	Turn-off propagation delay	V_S = 600V		150	220	ns
t_r	Turn-on rise time			70	170	ns
t_f	Turn-off fall time			35	90	ns
t_{DM}	Delay matching				50	ns

NOTE4 *The V_{IN}, V_{TH}, and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output pins: HO and LO.*

Timing Waveforms

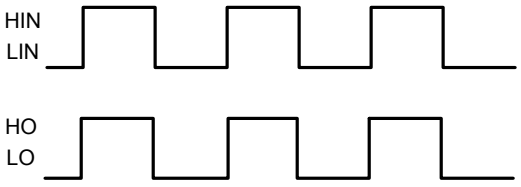


Figure 1. Input / Output Timing Diagram

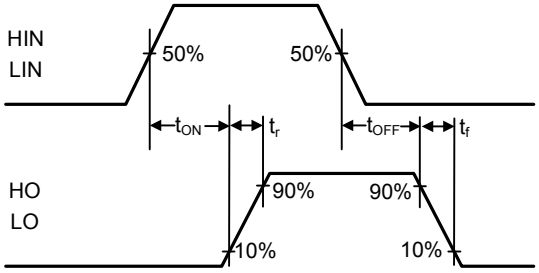


Figure 2. Switching Time Waveform Definitions

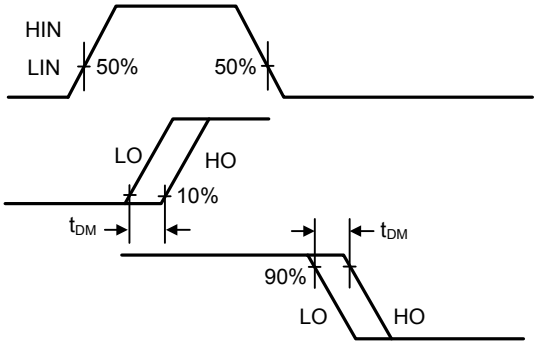


Figure 3. Delay Matching Waveform Definitions

Typical Characteristics

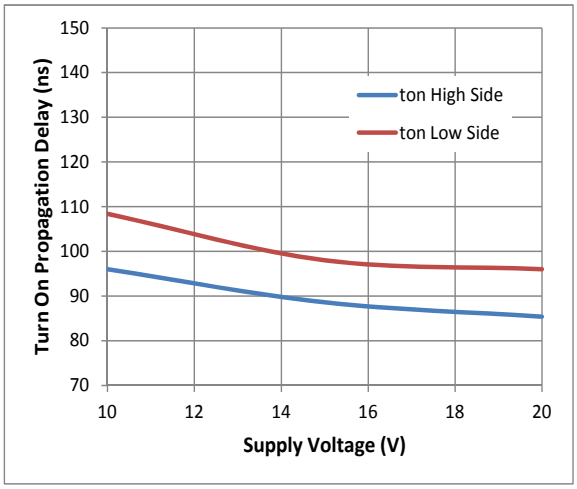


Figure 4. Turn-on Propogation Delay vs. Supply Voltage

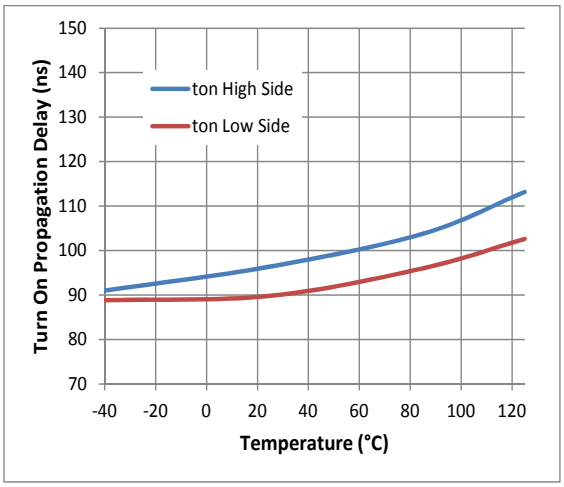


Figure 5. Turn-on Propogation Delay vs. Temperature

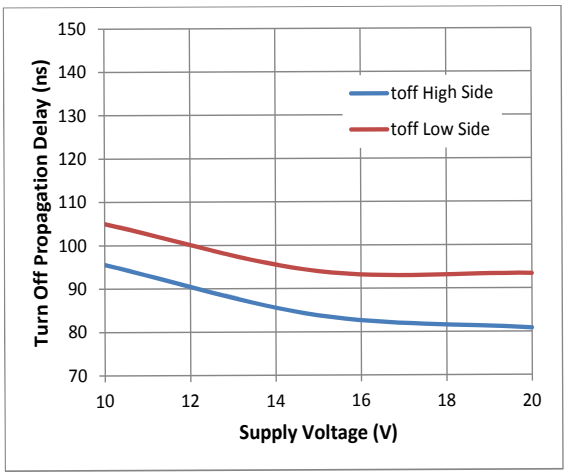


Figure 6. Turn-off Propogation Delay vs. Supply Voltage

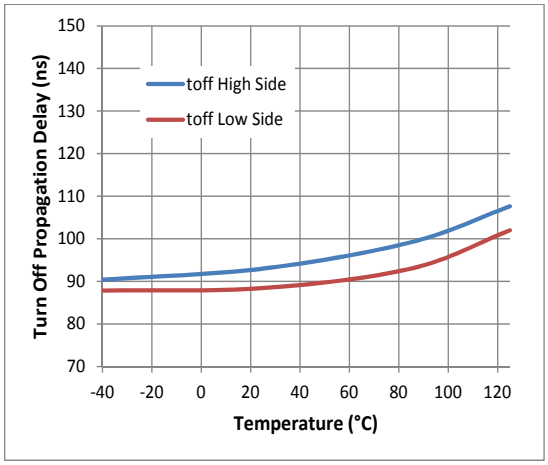


Figure 7. Turn-off Propogation Delay vs. Temperature

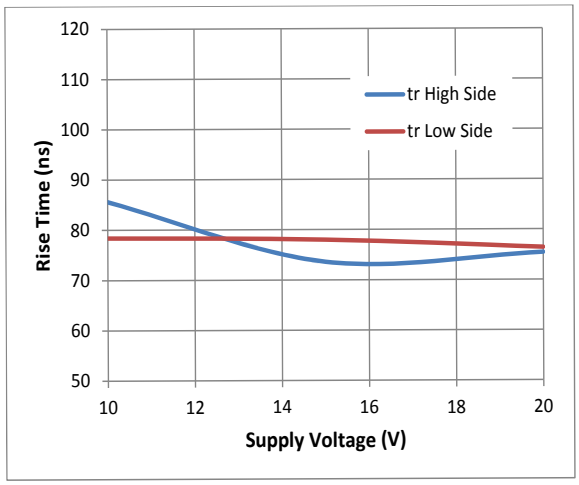


Figure 8. Rise Time vs. Supply Voltage

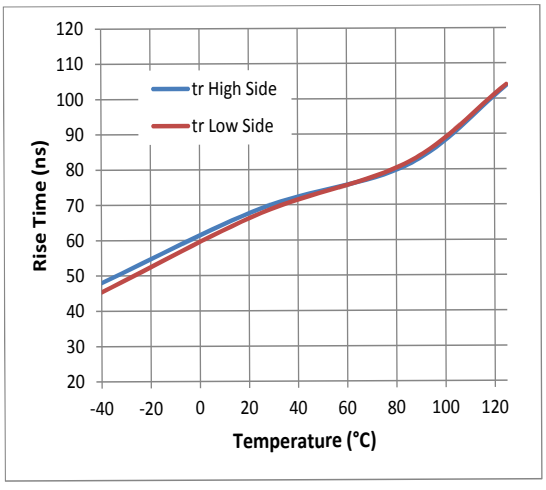


Figure 9. Rise Time vs. Temperature

Typical Characteristics, cont'd

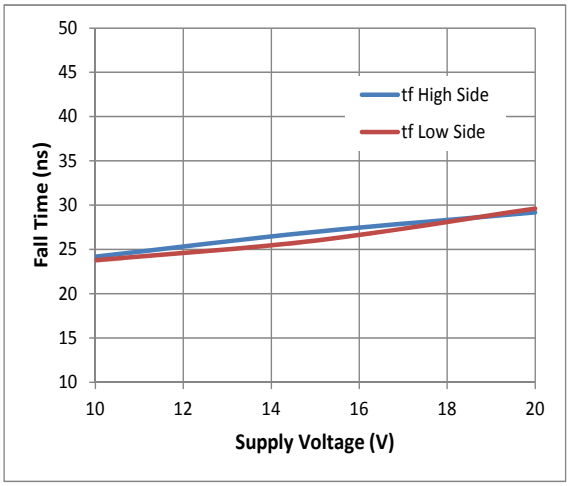


Figure 10. Fall Time vs. Supply Voltage

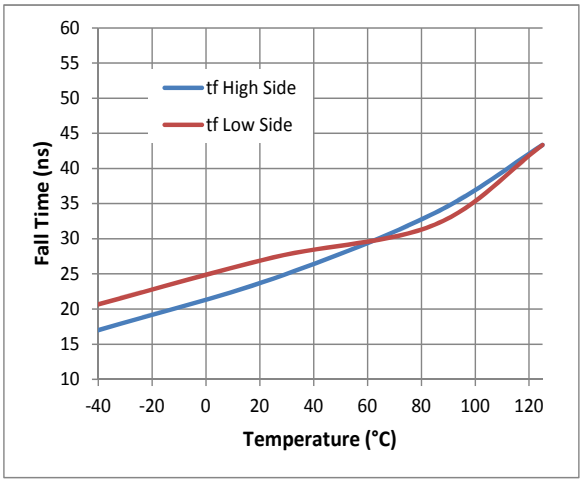


Figure 11. Fall Time vs. Temperature

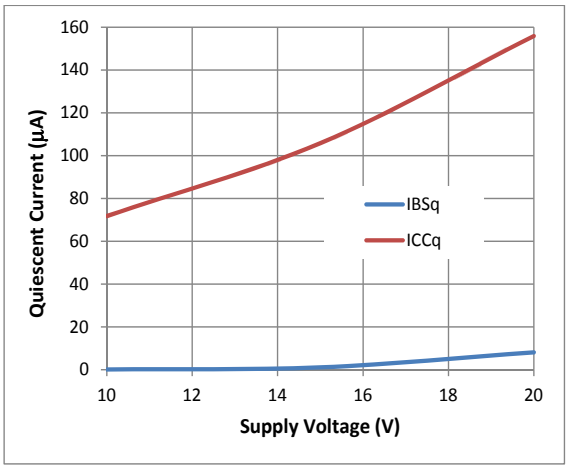


Figure 12. Quiescent Current vs. Supply Voltage

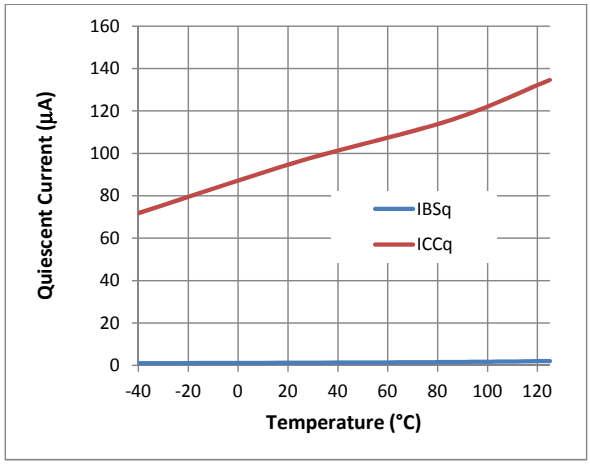


Figure 13. Quiescent Current vs. Temperature

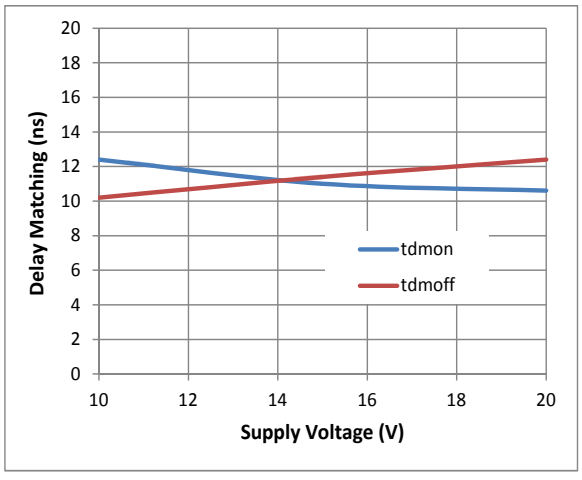


Figure 14. Delay Matching vs. Supply Voltage

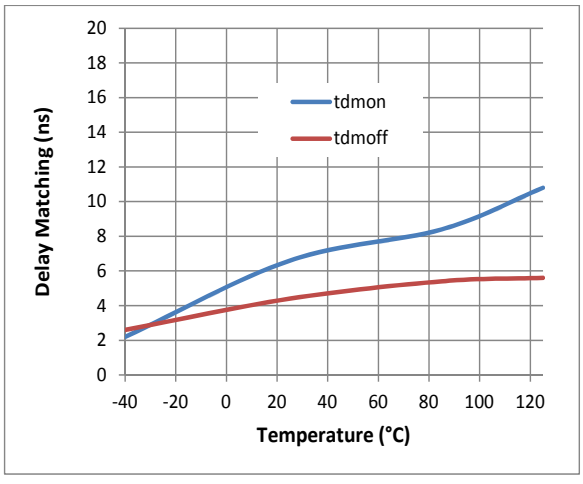


Figure 15. Delay Matching vs. Temperature

Typical Characteristics, cont'd

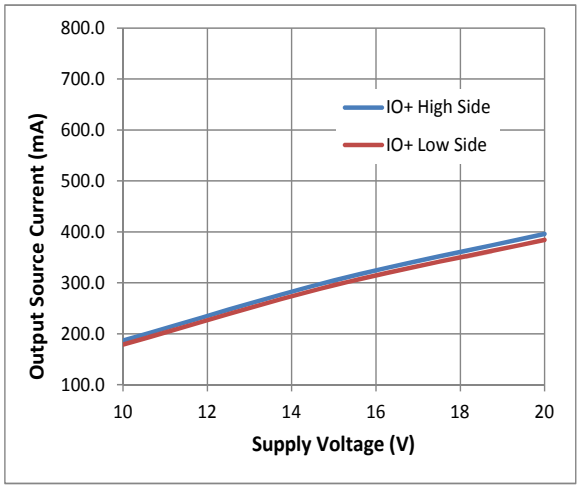


Figure 16. Output Source Current vs. Supply Voltage

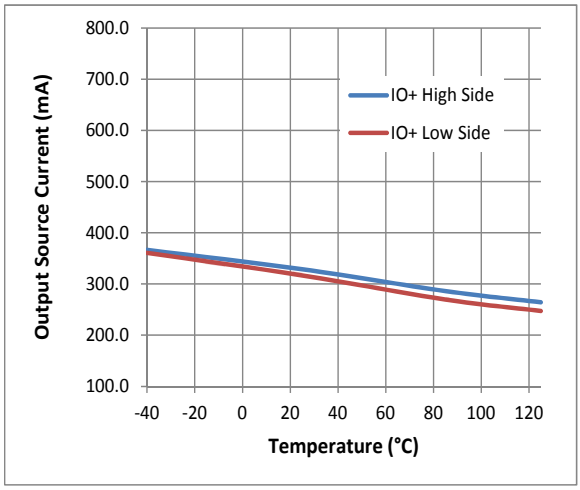


Figure 17. Output Source Current vs. Temperature

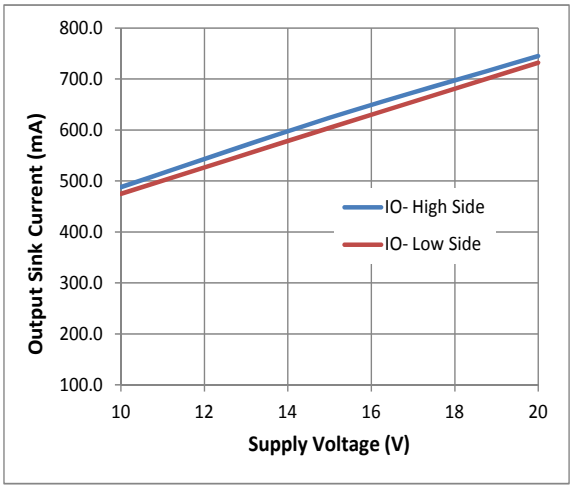


Figure 18. Output Sink Current vs. Supply Voltage

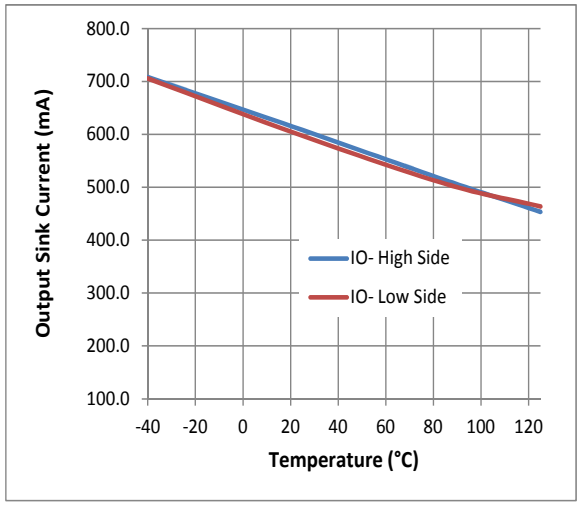


Figure 19. Output Sink Current vs. Temperature

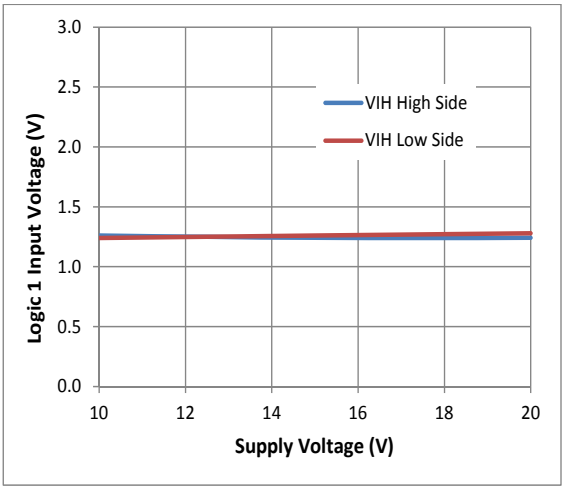


Figure 20. Logic 1 Input Voltage vs. Supply Voltage

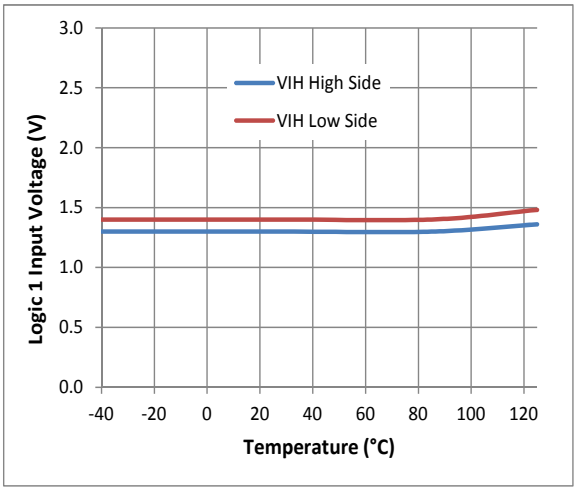


Figure 21. Logic 1 Input Voltage vs. Temperature

Typical Characteristics, cont'd

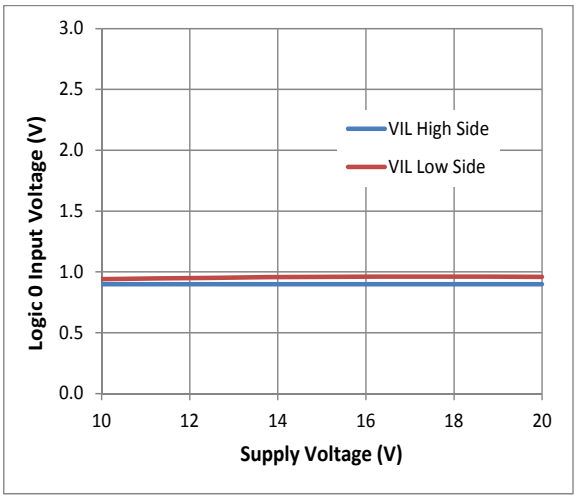


Figure 22. Logic 0 Input Voltage vs. Supply Voltage

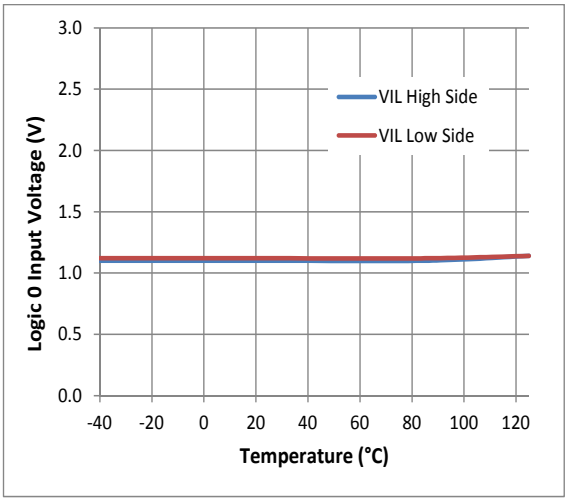


Figure 23. Logic 0 Input Voltage vs. Temperature

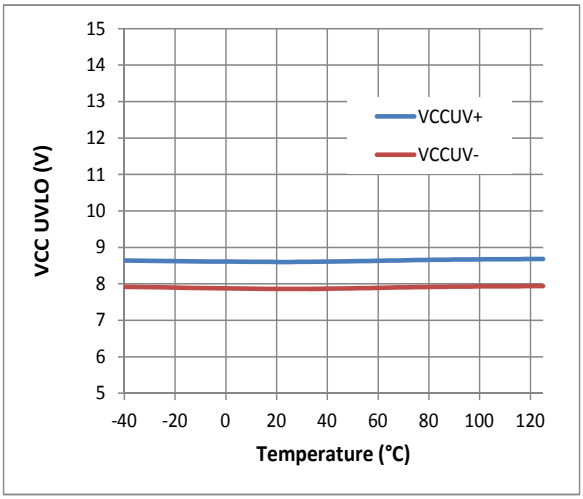


Figure 24. V_{CC} UVLO vs. Temperature

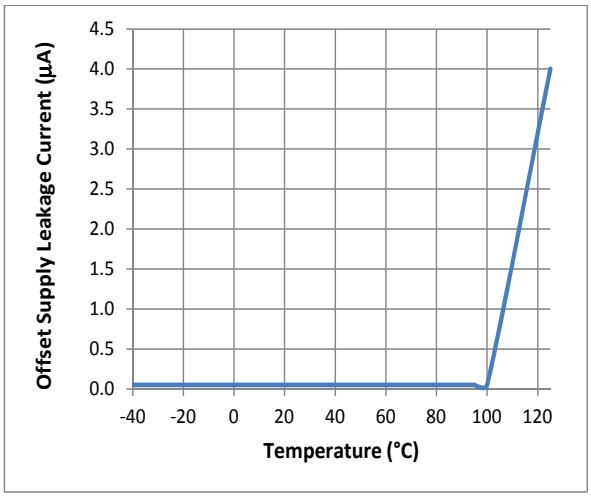
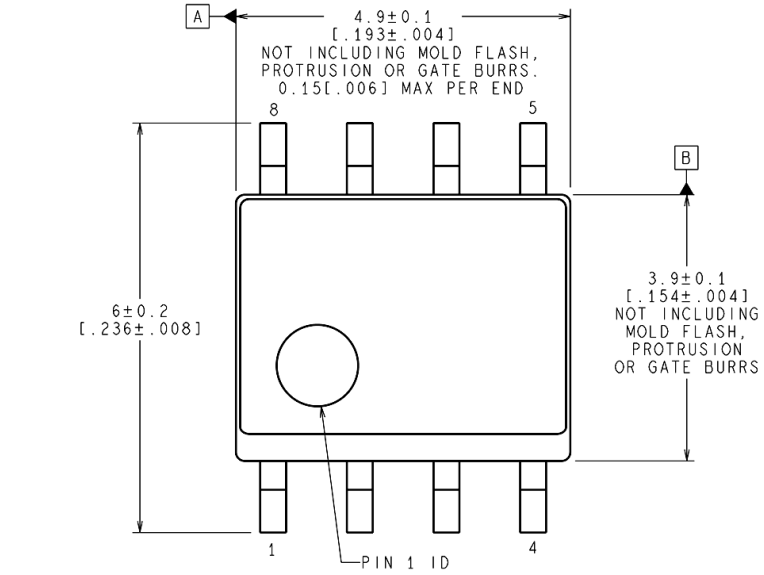
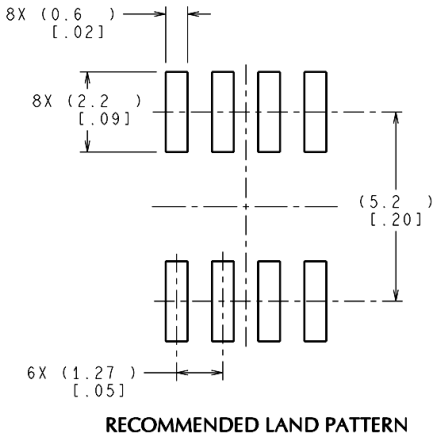


Figure 25. Offset Supply Leakage Current Temperature

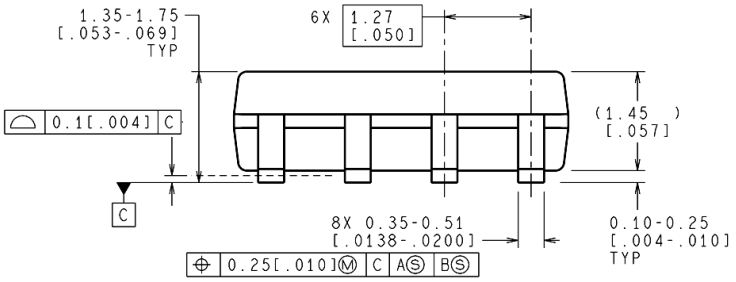
Package Dimensions (SOIC-8 N)

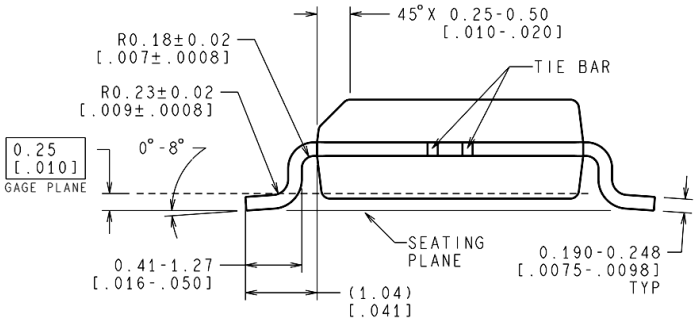
Please contact support@tfsemi.com for package availability.





RECOMMENDED LAND PATTERN





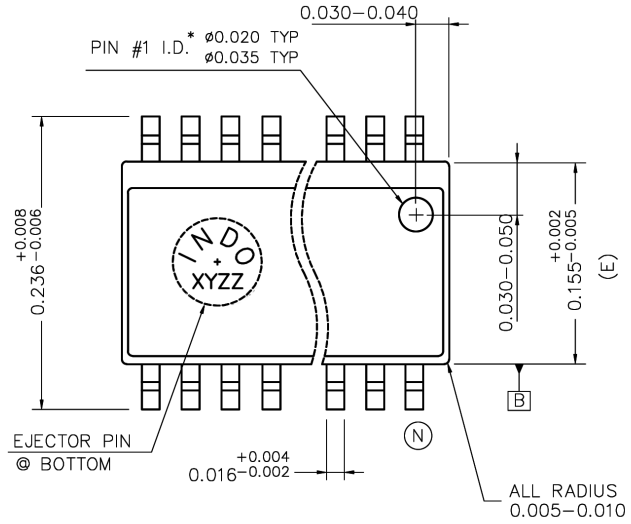
NOTES: UNLESS OTHERWISE SPECIFIED

1. REFERENCE JEDEC REGISTRATION MS-012, VARIATION AA.

CONTROLLING DIMENSION IS MILLIMETER
VALUES IN [ ] ARE INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

Package Dimensions (SOIC-14 N)

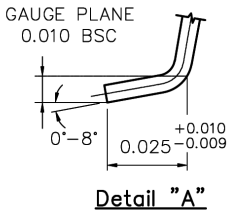
Please contact support@tfsemi.com for package availability.



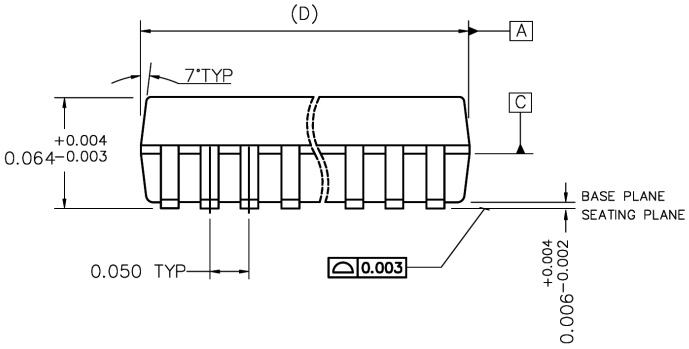
ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE NOTED

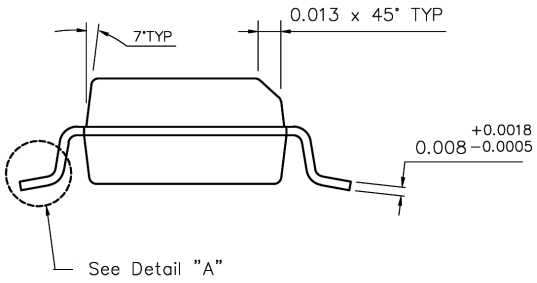
NOTES:

1. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSION. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 6 MILS PER SIDE.
2. "N" IS THE NUMBER OF TERMINAL POSITIONS.
3. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 3 MILS (Ⓒ SEATING PLANE) OUTGOING ASSEMBLY & 4 MILS AFTER TEST.
4. THE BOTTOM PACKAGE LEAD SIDE MAY BE BIGGER THAN THE TOP PACKAGE LEAD SIDE BY 4 MILS (2 MILS PER SIDE). BOTTOM PACKAGE DIMENSION SHALL FOLLOW DIMENSION STATED IN THIS DRAWING.
5. THE BOTTOM EJECTOR PIN CONTAINS COUNTRY OF ORIGIN "INDO" AND MOLD ID. (REFER TO TABLE FOR OPTION).
6. THIS DRAWING CONFORMS TO JEDEC REF. MS–012 REV. E

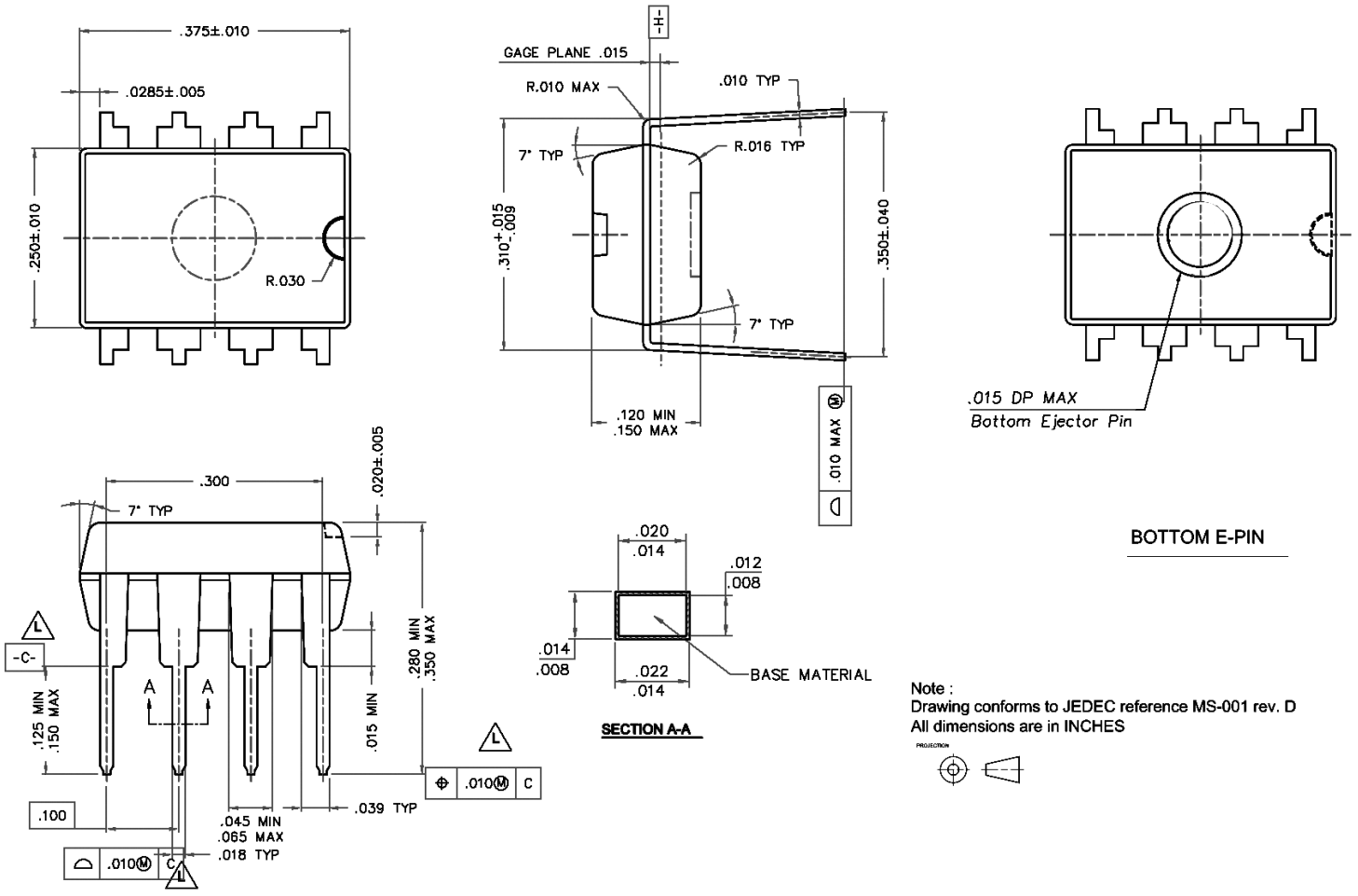


N	D VARIATION			MGP MOLD			
				STANDARD		MATRIX	
	MIN	NOM	MAX	PIN 1 I.D.	EJECT PIN	PIN 1 I.D.	EJECT PIN
08	0.189	0.193	0.196	N/A		YES	YES
14	0.337	0.339	0.344	YES	NO	YES	YES
⚠ 16	0.386	0.390	0.393	N/A		YES	YES





Package Dimensions (PDIP-8)



Notes

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